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B.Tech
BSCP1207

3rd Semester Back Examination 2016-17
PHYSICS OF SEMICONDUCTOR DEVICES
BRANCH(S): AEIE, CSE, ECE, EIE, ETC, IT, ITE
Time: 3 Hours
Max Marks: 70
Q.CODE:Y551
Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

- **a)** The electrons in crystals occupy certain allowed energy bands and are excluded from the forbidden energy bands. Name a model which predicts the above principle and write down the wave function describing it.
- **b)** Distinguish between direct band gap semiconductor and indirect band gap semiconductor.
- **c)** Calculate the co-efficient of diffusion for positive charge carriers in germanium at room temperature. The hole mobility for germanium may be taken as 1900cm^2/VS.
- **d)** Draw the plot of variation of E_F with doping concentration.
- **e)** Explain the variation of conductivity of semiconductor with temperature.
- **f)** Draw k-space diagrams of Si and GaAs.
- **g)** In what type of application of BJT, Hybrid-Pi model is used?
- **h)** What do you mean by carrier generation and recombination?
- **i)** What is the value of surface potential under flat band condition?
- **j)** What is pinch off voltage?

Q2

- **a)** Write the expression for probability function of electrons and holes in donor and acceptor energy states. Discuss complete ionization and freeze out conditions with suitable energy band diagrams. **(5)**
- **b)** The forbidden energy gap in silicon is 1.1eV. The effective density of states both in conduction band and valence band is assumed to be $2.41 \times 10^{19} cm^{-3}$. Calculate the intrinsic electron concentration in Silicon at room temperature. **(5)**

Q3

- **a)** Derive the expression for excess minority carrier electron concentration in the forward active mode in an npn transistor. **(5)**

b) Consider a uniformly doped silicon bipolar transistor at T = 300 K with a base doping of $N_B = 5 \times 10^{16} cm^{-3}$ and a collector doping of $N_C = 2 \times 10^{15} cm^{-3}$. Assume the metallurgical base width is 0.7 mm. Calculate the change in neutral base width as the collector-base voltage changes from 2 to 10 V. **(5)**

Q4

a) Define threshold voltage. Derive an expression for threshold voltage of a MOS capacitor. **(5)**

b) In certain experiment in semiconductor device laboratory, a student measure depletion layer capacitance C_d against reverse bias voltage V_R of a typical PN junction. She obtained a straight line on graph paper by taking $\frac{1}{C_d^2}$ along Y-axis and V_R along X-axis. The slope of the line was $2 \times 10^{23} F^{-2} V^{-1}$ and intercept was -0.84V. Calculate the doping concentrations in p-side and n-side of the pn junction if its cross-sectional area was $1.0 \mu m^2$. **(5)**

Q5

a) Derive an expression for built-in potential barrier of a uniformly doped abrupt pn junction in thermal equilibrium with necessary energy band diagram. **(5)**

b) For a Si pn junction, at T = 300K with zero applied bias has doping concentrations of $N_d = 6 \times 10^{16} cm^{-3}$ and $N_a = 4.5 \times 10^{15} cm^{-3}$. Determine x_n, x_p and space charge width W. Given $n_i = 1.5 \times 10^{10} cm^{-3}$, $\epsilon_s = 11.7\epsilon_0$ with $\epsilon_0 = 8.85 \times 10^{-14} C^2 N^{-1} cm^{-2}$. **(5)**

Q6

a) What is threshold inversion in a MOS capacitor? Derive the expression for Flat-band voltage of a MOS capacitor with p – type semiconductor substrate. **(5)**

b) Calculate the flat band voltage for an MOS capacitor with a p-type semiconductor substrate doped to $N_a = 10^{16} cm^{-3}$, a silicon dioxide insulator with a thickness of $t_{ox} = 200 A^0$, an n+ poly-silicon gate and an oxide charge of $Q_{ss}^{'} = 8 \times 10^{10} cm^{-2}$. **(5)**

Q7

a) Derive the expression for induced electric field for a non-uniformly doped n – type semiconductor and the Einstein's relation between diffusion co-efficient and mobility. **(5)**

b) What do you mean by CMOS technology? Sketch the cross section of a CMOS structure. Discuss what is meant by latch-up in a CMOS structure. **(5)**

Q8 **Write short notes on any two of the followings:** **(5 x 2)**

a) MOSFET V_T and Body effect.

b) Breakdown mechanism in Transistor.

c) N-Channel MOSFET and P-Channel MOSFET.

d) C-V Characteristics of MOS Capacitor.