Registration No. : | | | | | | | | | | |

Total number of printed pages – 4

B.Tech
BE 2101

Second Semester Examination – 2012

BASIC ELECTRONICS

Full Marks – 70

Time : 3 Hours

*Answer Question No. **1** which is compulsory and any **five** from the rest.*
Symbols carry their usual meaning.
The figures in the right-hand margin indicate marks.

1. Answer the following questions in brief : 2×10

   (a) What do you mean by frequency spectrum ? Calculate the frequency and time period of the following sinusoidal signal $f(t) = 5\sin(300t)$.

   (b) A diode is operated at room temperature with $I_s = 10^{-10}$ A and $\eta = 2$. (i) What is the diode current i_D if the voltage across the diode is $V_D = 0.65$ V ? (ii) What voltage V_D is required for a diode current of 200 μA ?

   (c) A BJT has a base current of $i_B = 5$ μA and a gain of $\beta_F = 150$ V/V. (i) If the BJT is operating in the forward active region, and ignoring the effect of V_A, what is the value of the collector current i_C ? (ii) If $V_A = 75$ V, what is i_C at $V_{CE} = 5$ V ?

   (d) Define 'CMRR'. If the CMRR of an Op-Amp is 80 dB and the common mode gain is –0.5, what is the differential mode gain of the Op-Amp ?

   (e) Why time-base is used in a Cathode Ray Oscilloscope ?

   (f) A silicon sample at room temperature is doped with acceptor atoms so that $N_A = 10^{16}$ cm^{-3} and $N_D = 0$. Is the material p-type or n-type ? If $p_0 = 10^{16}$ cm^{-3}, what is the electron concentration, n_0 at room temperature ?

   (g) Convert $(10.01)_{10}$ to its equivalent binary number.

P.T.O.

(h) Prove that : (i) $X + \overline{X}Y = X + Y$, (ii) $AB + \overline{A}B + A\overline{B} + \overline{A}\overline{B} = 1$.

(i) What is the upper and lower limit of a DC load line for a fixed bias circuit ?

(j) With the help of a suitable example show how negative feedback increases the bandwidth of an amplifier by a factor of $(1 + \beta A_0)$, where β is the feedback factor and A_0 is the mid-band gain without feedback.

2. In a fixed bias circuit with emitter stabilized resistor, $R_B = 560\ k\Omega$, $R_C = 4.7\ k\Omega$, $R_E = 1\ k\Omega$, $V_{CC} = 10\ V$, $\beta = 80$, coupling capacitors of 0.01 μF and $C_E = 0.047\ \mu F$ are used.

(a) Draw the circuit diagram and find the values of V_{CEQ} and I_{CQ}. 4

(b) Draw the low frequency small signal hybrid-π equivalent model and determine the value of g_m and r_π. (Assume room temperature for your calculations). 3

(c) Determine A_V and Z_i for the circuit. 3

3. (a) Consider the half-wave rectifier circuit shown in Figure 3 (a) below. If V_{in} is a triangle wave with a peak voltage of 2 V, and the diode has $V_d = 0.5\ V$, sketch V_{out} as a function of time on the plot of V_{in} shown in Figure 3 (a) below. Label the peak voltage of V_{out}. 3

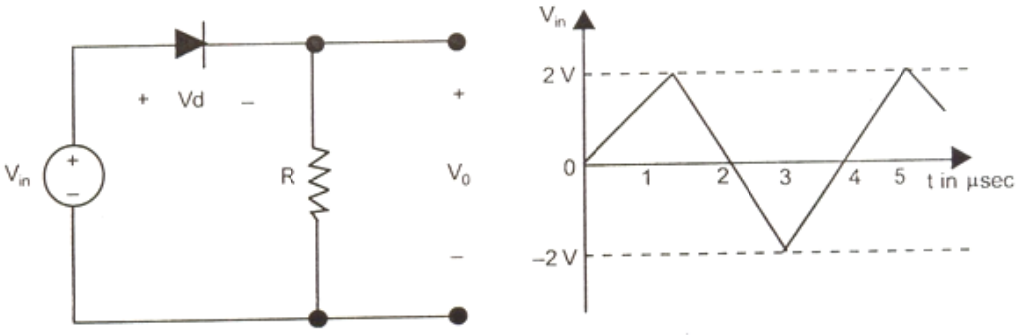

Figure 3 (a)

(b) For the circuit given in Figure 3(b) below, draw the output wave form for the input as shown. Assume the diodes to be ideal. 4

Given: $V_{R1} = 2$ V and $V_{R2} = 3$ V.

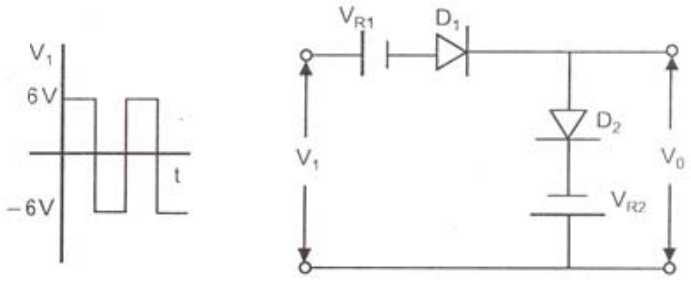

Figure 3 (b)

(c) At room temperature, the diode in Figure 3(c) below has the model parameters $I_S = 10^{-9}$ A and $\eta = 2$. The dc voltage source has the value $V_1 = 2$ V. The source labeled v_1 puts out a sinusoidal voltage and can be considered to be a small-signal source. For $v_1 = 0$ V, solve for the value of R_1 which biases the diode at $I_D = 2$ mA. 3

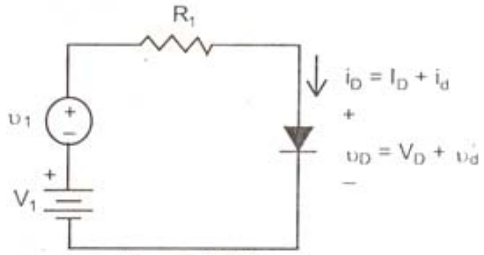

Figure 3(c)

4. Design a potential divider stable bias circuit as shown in the Figure 4 below with a Q point of $I_C = 25$ mA and $V_{CE} = 7.5$ V. Transistor β ranges from 50 to 200. 10

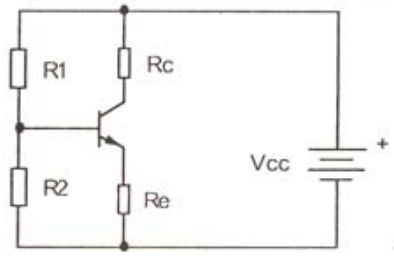

Figure 4

5. For an instrumentation amplifier of the type shown in Figure 5 below, a designer proposes to make $R_2 = R_3 = R_4 = 100\ k\Omega$, and $2R_1 = 10\ k\Omega$. For ideal components, calculate the difference-mode gain, common-mode gain and CMRR. If we change $2R_1 = 1\ k\Omega$ what value of difference-mode gain, common-mode gain and CMRR result ? 10

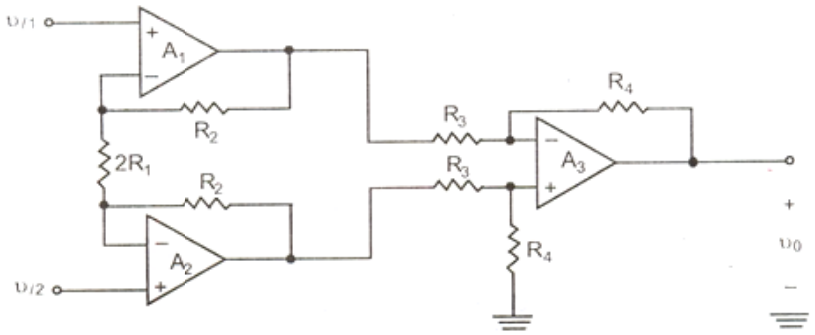

Figure 5

6. (a) Simplify the following Boolean expression and draw its logic circuit : 5

$A'BC + AB'C' + A'B'C' + AB'C + ABC.$

(b) Design a combinational logic circuit which adds three binary bits and implement using NAND gates. 5

7. (a) With neat diagram, describe the operation of Wien Bridge Oscillator. 6

(b) Define Multiplexing and Demultiplexing. How many 8 × 1 multiplexers are used to design a 64 × 1 multiplexer ? 4

8. Answer any **two** of the following : 5×2

(a) AF signal generator

(b) SR latch

(c) BJT as a switch

(d) Feedback amplifier.