GIET Main Campus (Autonomous)
Gunupur-765 022

Reg.No.: | | | | | | | | | | | | |

B.TECH. DEGREE EXAMINATION-NOV-DEC.2018
End Semester Examination
BELPC3020/BEEPC3030-Analog and Digital Circuits
(Regulations 2017)(Common to EE and EEE Branches)

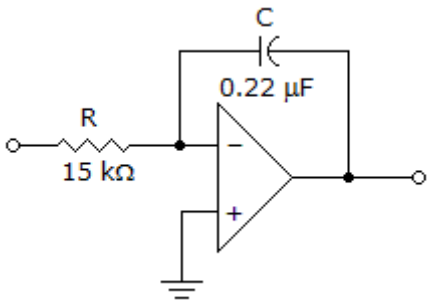
Time : 3 Hours **Maximum : 100 Marks** **Question Code:301012**
Answer ALL Questions

PART A - (10 X 2 = 20 Marks)

1. (a) Calculate minority current ICO if IC = 20.002 mA and IC majority = 20 mA [CO1][PO2]
   A. 20 A
   B. 0.002 A
   C. 2 nA
   D. 2 A

   (b) For normal operation of a pnp BJT, the base must be.....with respect to the emitter and..... with respect to the collector. [CO1][PO1]
   A. positive, neg B. positive, positive
   C. negative, positive
   D. negative, negative

   (c) Refer to the given figure. A square-wave input is applied to this amplifier. The output voltage is most likely to be [CO2][PO2]



   A. a square wave.
   B. a triangle wave.
   C. a sine wave.
   D. no output.

   (d) In which of the following are operational amplifiers (op-amps) used? [CO2][PO1]
   A. Oscillators
   B. Filters

C. Instrumentation circuits
D. All of the above

(e) Why an integrator cannot be made using low pass RC circuit? [CO2][PO1]
A. It require large value of R and small value of C
B. It require large value of C and small value of R
C. It require large value of R and C
D. It require small value of R and C

(f) In the decimal numbering system, what is the MSD? [CO3][PO1]
A. The middle digit of a stream of numbers
B. The digit to the right of the decimal point
C. The last digit on the right
D. The digit with the most weight

(g) Convert hexadecimal value 16 to decimal. [CO3][PO2]
A. 2210
B. 1610
C. 1010
D. 2010

(h) How many bits are in an ASCII character? [CO3][PO1]
A. 16
B. 8
C. 7
D. 4

(i) How much storage capacity does each stage in a shift register represent? [CO4][PO1]
A. One bit
B. Two bits
C. Four bits
D. Eight bits

(j) Latches constructed with NOR and NAND gates tend to remain in the latched condition due to which configuration feature? [CO4][PO1]
A. Low input voltages
B. Synchronous operation
C. Gate impedance
D. Cross coupling

PART B - (10 X 2 = 20 Marks)

2. (a) Explain why an ordinary junction transistor is called bipolar? [CO1][PO1]

(b) What is the difference between BJT and FET? [CO1][PO1]

(c) Define slew rate. [CO2][PO1]

(d) Define CMRR [CO2][PO1]

(e) Calculate the output voltage of a non inverting amplifier for values of V1 = 2 V, Rf = 500 kΩ, and R1 =100 kΩ. [CO2][PO2]

(f) Convert the hexadecimal number 4AC7. 4B into its equivalent octal number [CO3][PO2]

(g) Find the gray equivalent of the following binary numbers: 100010111 [CO3][PO2]

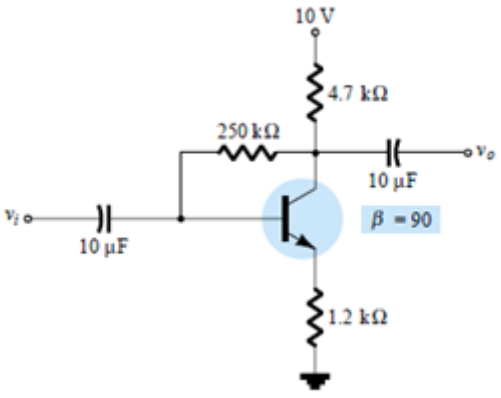
(h) Write the expression in SOP form, $y = AB + C$ [CO3][PO2]

(i) If an 8-bit ring counter has an initial state 10111110, what is the state after the fourth clock pulse? [CO4][PO2]

(j) Write the excitation table for JK and SR flip flop. [CO4][PO1]

PART C - (4 X 15 = 60 Marks)

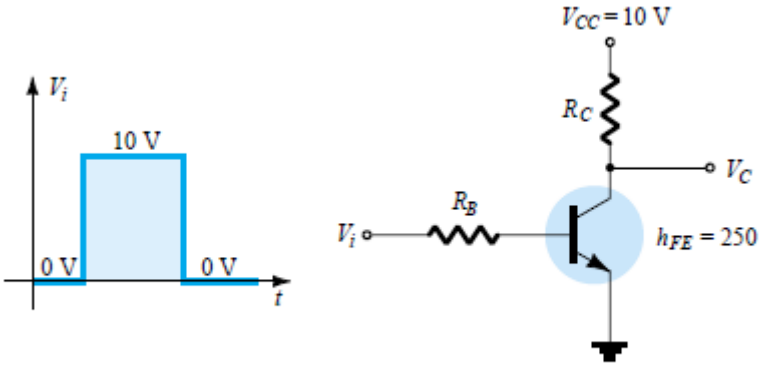
3. (a) (i) Determine the quiescent levels of ICQ and VCEQ for the network of Fig [10][CO1][PO2]



(ii) Write short note on working principle of photovoltaic cell [5][CO1][PO1]

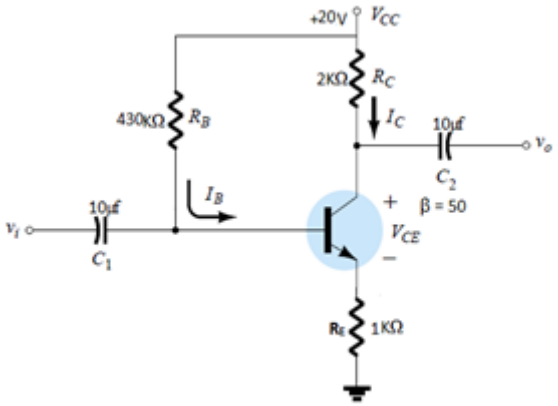
(or)

(b) (i) Determine RB and RC for the transistor inverter of Fig. if ICsat $_1 0mA$. [7][$CO1$][$PO2$]



(ii) For the emitter bias network of Fig., determine: [8][CO1][PO2]

(a) IB.
(b) IC.
(c) VCE.
(d) VC.
(e) VE.
(f) VB.
(g) VBC.



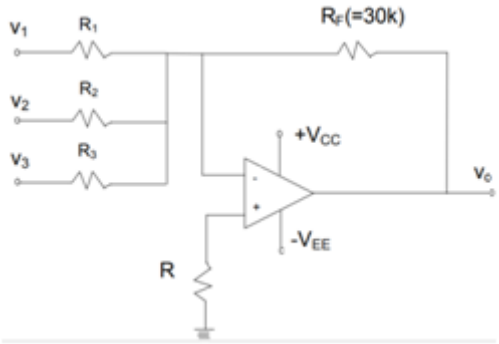
4. (a) (i) Determine the output voltage of an op-amp for input voltages of Vi1 = 150 μ V, Vi2 =140 μV. The amplifier has a differential gain of Ad = 4000 and the value of CMRR is: [8][CO2][PO2]

(a) 100. (b) 10 5 15 Marks CO2 PO2 8

(ii) Derive an expression for op-amp as differentiator with an example. [7][CO2][PO2]

(or)

(b) (i) For the summing amplifier shown in fig., estimate the values of resistors R1,R2 and R3 so that the output Vθ is, Vθ = - (3V1 + V2 + 0.2V3) What is the approximate value of the compensating resistor R? [8][CO2][PO2]



(ii) Derive an expression for op-amp as integrator with an example. [7][CO2][PO2]

5. (a) (i) Design a logic gate for BCD to binary code conversion. [8][CO3][PO3]

(ii) Design a full adder using 1:8 DMUX. [7][CO3][PO2]

(or)

(b) (i) Design a 8:1 mux using two 4:1 mux and one 2:1 mux [7][CO3][PO3]

(ii) Design the following three variable expression F(A,B,C)=Σ(0,1,5,7,13,14) Using 1:8 DMUX [8][CO3][PO3]

6. (a) (i) Represent T flip flop in terms of JK flip flop [7][CO4[PO2]

(ii) Write the working principle of universal shift resister [8][CO4[PO2]

(or)

(b) (i) Explain about serial input serial output shift resister [8][CO4[PO3]

(ii) Design a asynchronous MOD-10 counter [7][CO4[PO3]