Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**
FECE6401

7th Semester Back Examination: 2018-19
COMPUTER SYSTEM ARCHITECTURE
BRANCH:AEIE, ECE, EIE, ETC, IEE
Time: 3 Hours
Max Marks: 70
Q.CODE:E255
Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) "Hardwired control unit is faster than micro programmed control unit." Justify this statement.
b) What are the limitations of Booth's algorithm? Write down its significance to computer performance.
c) Registers R1 and R2 of a computer contain the decimal values 1200 and 4600. What is the effective address of the memory operand in each of the following instructions?
i) Load 20 (R1),R5 ii) Add -(R2),R5
d) Define the two parameters responsible for single/multi block data transfer between memory and processor to have better computer system performance.
e) Consider an SDRAM with refreshing period of 64 ms, with its cells arranged in 8K rows and takes four clock cycles to read each row. Find out the refresh overhead at a clock rate of 133 MHz.
f) State the different types of operations that must be supported by the instructions of the computer.
g) What is a Program Counter? State the role of the program counter in adressing.
h) Write down one example for i) One address instruction ii) Two address instructioniii) Three address instruction iv) Four address instruction, each.
i) Define the two types of byte addresses used for word assignment in commercial machines.
j) How many 128x8 RAM using chips are needed to provide a memory capacity of 2048 bytes?

Q2 **a)** Explain the concept of Memory interleaving with suitable diagram. **(5)**
b) Write short notes on :i) Microinstruction ii) Micro-program sequencer **(5)**
What do you mean by Wide-branch addressing? Explain with example

Q3 **a)** What is Stack organization? Compare register stack and memory stack. **(5)**
b) What is ROM? How does PROM differs from EEPROM. **(5)**

Q4 **a)** Define the basic format used to represent the floating-point numbers. Also define the concept of normalization and biasing with some examples. **(5)**
b) Show the step by step process of Booth's multiplication algorithm with the help of a flowchart and perform multiplication of (-13) and (-8) using Booth's algorithm. **(5)**

Q5 **a)** Briefly explain high – speed adder? Discuss design of high speed adders. **(5)**

b) What do you mean by Bus and explain bus interconnection. **(5)**

Q6 **a)** A virtual memory has page size of 1 K words. There are 8 pages and 4 blocks. The associative memory page table contains the following entries: **(5)**

Page	Block
0	3
1	1
4	2
6	0

Find a list of all virtual addreses (in decimal) that will cause a page fault if used by CPU.

b) Write an assembly language program to evaluate the arithmetic statement : **(5)**
E = (A + B) / (C – D) * F
Using :
a) General register computer with three address instruction.
c) Using an accumulator type computer with one address instruction.

Q7 Explain direct mapping, associative mapping, and set associative mapping with suitable diagrams? What is the benefit of using a cache memory with L1 and L2 cache? Give example in support of your answer. **(10)**

Q8 **Write short answer on any TWO:** **(5 x 2)**

a) Hardwired control unit
b) Address, data and instruction register.
c) Stack based processor organization
d) Horizontal and vertical microinstruction formats.