Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PCEC4401

7th Semester Back Examination 2018-19
VLSI DESIGN
BRANCH : AEIE, BIOMED, CSE, ECE, EEE, EIE, ELECTRICAL, ETC, IEE, IT, ITE
Time : 3 Hours
Max Marks : 70
Q.CODE : E431

Answer Question No.1 which is compulsory and any FIVE from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions :** **(2 x 10)**

a) What is standard cell-based design methodology?
b) What is Design Hierarchy?
c) What is Twin-tub process? Why it is called so?
d) When the channel is said to be pinched off?
e) With the help of a neat sketch show and explain various terms like channel length (L), lateral diffusion length (L_D), and effective channel length (L_{eff}) for a MOS transistor.
f) What is the minimum power supply voltage required for a CMOS inverter so that it can operate properly?
g) Design a resistive load inverter using enhancement ***n***MOS as a driver to get $V_{OL} = 0.3\,V$. Given parameters for the MOS transistor are: V_{T0} = 1V, $\mu_n C_{ox}$ = 50 $\mu A/V^2$. Take R_L = 10 KΩ and V_{DD} = 5 V.
h) Why the pull-up network is replaced with a single ***p***MOS transistor in pseudo-***n***MOS logic?
i) Implement a 2-input NAND gate using pass transistor logic.
j) In a DRAM what is the main significance to precharge the bit-lines up to $V_{DD}/2$ instead of V_{DD}?

Q2 **a)** Calculate the zero-bias threshold voltage (i.e., for $V_{SB} = 0$) for an NMOS silicon-gate transistor that has well doping $N_A = 3\times10^{17}\ \text{cm}^{-3}$, gate doping $N_D = 10^{20}\ \text{cm}^{-3}$, gate oxide thickness $t_{ox} = 22\ \overset{0}{\text{A}}$, and $2\times10^{10}\ \text{cm}^{-2}$ singly charged positive ions per unit area at the oxide-silicon interface. Assume that the gate doping is n^+ and explain why it is appropriate. Calculate the ion-implant doses N_i (in unit of ions/cm^2) needed to achieve a threshold voltage of 0.4V. **(5)**

b) Explain the important process sequence for CMOS integrated circuit fabrication with the help of neat diagrams. **(5)**

Q3 **a)** Compare two technology scaling methods, namely, (i) the constant electric fielding scaling and (ii) the constant power supply voltage scaling. In particular, show analytically by using equations how the delay time ,power dissipation, and power density are affected in terms of scaling factor ,S. **(5)**

b) Calculate the diffusion parasitic capacitance C_{db} of the drain of a unit-sized contacted ***n***MOS transistor in a 180 nm process when the drain is at 0 V and at V_{DD} = 1.8 V. Assume the substrate is grounded. The transistor characteristics are C_J = 0.98 fF/ μm^2, M_J = 0.36, C_{JSW} = 0.22 fF/ μm, C_{JSWG} = **(5)**

0.33 fF/ μm, $M_{JSW} = M_{JSWG} =$ 0.10 and $\psi_0 =$ 0.75 V at room temperature.

Q4 **a)** Consider a CMOS inverter with the following parameters: **(5)**
$nMOSV_{TO,n}$= 0.6v $\mu_n C_{ox}$=60μA/V^2 $(W/L)_n$=8
$pMOSV_{TO,p}$=-0.7v $\mu_p C_{ox}$=25μA/V^2 $(W/L)_p$=12
Calculate the noise margins and the switching threshold (V_{th}) of this circuit.
The power supply voltage is VDD=3.3V.

b) In a CMOS inverter, assume that K'_n=20μA/V^2,$(W/L)_n$=10/1, K'_p=0.4 K'_n,$(W/L)_n$=10/1 and V_{DD}=5V.The inverter drives a load capacitance of 150fF. **(5)**
a) Find high -to -low propagation delay?
b) Find low –to-high propagation delay?
What should be the dimension of the PMOS transistor such that both are to be equal? Ignore the effect of PMOS transistor's size on the load capacitance of the Inverter

Q5 **a)** Draw the circuit diagram and the corresponding stick diagram of the logic gate computing the function $Y = \overline{(A + B + C) \cdot D}$ using CMOS technology. **(5)**

b) Draw and explain working of CMOS SR latch using positive logic and negative logic. Why edge triggered flip-flops are preferred? **(5)**

Q6 **a)** Discuss the charge sharing problems in VLSI circuits. Explain various circuit techniques used in domino CMOS circuits for solving charge sharing problems. State as many as you know. **(5)**

b) With the help of a neat circuit diagram show the implementation of the logic function $Y = \overline{(A \cdot B \cdot C) + (D \cdot E)}$ using dynamic CMOS logic. **(5)**

Q7 Draw the circuit structure/topology of the CMOS RAM cell. Explain its design strategy. Explain voltage levels in the SRAM cell at beginning of "read" operation and "write" operation. Show the corresponding timing diagram. **(10)**

Q8 **Write short answer on any TWO :** **(5 x 2)**

a) VLSI Layout Design Rules
b) Leakage currents in DRAM and SRAM cells
c) *Gajski's Y-chart*
d) Built-In Self-Test (BIST) Techniques