Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**

PCS5I101

5th Semester Regular / Back Examination 2018-19

OPERATING SYSTEMS

BRANCH : CSE

Time : 3 Hours

Max Marks : 100

Q.CODE : E097

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 **Short Answer Type Questions (Answer All-10)** **(2x10)**

a) What are the Real-time Systems? Give example.

b) What is Dispatcher? How it works with the scheduler?

c) Enlist the reasons behind the process suspension.

d) What is starvation and aging?

e) Which factors determine whether a detection-algorithm must be utilized in a deadlock avoidance system?

f) What Is Spooling?

g) How critical section problem can be solved?

h) When Does Thrashing Occur?

i) What Is Root Partition?

j) What differences are there between a semaphore wait signal and a condition variable wait signal?

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any EIGHT out of TWELVE)** **(6x8)**

a) Define a system call? List the different types of the system calls.

b) Explain the structure of the operating systems.

c) What is the Process Control Block? List its fields.

d) If the address bit is associated with a memory 25 bit, find out the total memory capacity. What are the strategies required for memory management?

e) Define context switching. Explain the process schedulers used in process scheduling.

f) State and explain Banker's algorithm.

g) Consider Logical Address Space is 256mb, Physical Address is 25 bits, offset field contains 13 bits. Find out page size, no of frames, no of pages.

h) What is thrashing? Why does it occur? How the deployment of working-set model can prevent thrashing?

i) Explain paging technique with TLB. Find out the hit ratio required to reduce the effective memory access time of 200 ns without TLB to 140 ns with TLB. Assume TLB access time is 25 ns.

j) Design the RAID structure and explain briefly.

k) Explain cycle stealing method and IPC mechanism.

l) What are the methods for free space management.

Part-III

Long Answer Type Questions (Answer Any TWO out of FOUR)

Q3 Enlist the different criterias of CPU scheduling. **(16)**
Consider the set of processes are P0, P1, P2, P3, P4, P5 with arrival time(sec.) 5,6,4,0,9 with burst time(sec.) 5,10,2,6,5. Calculate the waiting time and turn around time of each process & average waiting time.

Q4 What are the necessary conditions for arising deadlocks? How can you avoid and recover from deadlocks? **(16)**

Q5 Describe the method of Demand Paging. Explain the page replacement algorithms - FIFO, LRU, and Optimal. Suppose main memory has 3 frames & page nos which are going to be referenced are 1,1,3,2,2,2,4,9,9,6,3,2,2,7,6,6,3,3. Find out total page fault and page hit using each algorithm. **(16)**

Q6 What are the factors that determine the effective use of disk, Explain? **(16)**
Required blocks which are going to be accessed from a disk drive are on the cylinder 98,183,37,122,14,124,65,67. Disk head is initially at cylinder 53.Find out total no of head movements using each algorithm.