Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**

PET5H002

5th Semester Regular / Back Examination 2018-19

DIGITAL VLSI DESIGN

BRANCH : ECE, ETC

Time : 3 Hours

Max Marks : 100

Q.CODE : E226

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 **Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) What are the typical values of threshold voltage for nMOS and pMOS respectively?

b) What do you understand by W/L ratio? Why it is an important parameter in designing CMOS based circuits?

c) Define the terms Modularity and Locality.

d) Name the different capacitances associated with a MOS.

e) Draw a dominoCMOS circuit diagram for a NAND2 gate.

f) Draw a circuit diagram of NOR2 gate using transmission gates.

g) What do you understand by switching power dissipation of CMOS based circuits?

h) What is a pass transistor? Mention the limitations of these.

i) What do you understand by LOCOS in context of fabrication technology?

j) What is stuck-at fault?

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any EIGHT out of TWELVE)** **(6 x 8)**

a) Draw a neat and properly labelled diagram of Y-chart describing various design domains. Explain the diagram sufficiently.

b) Compare and contrast between constant field and constant voltage scaling methods in terms of area, power and delay parameters.

c) Draw a circuit diagram for a two input Ex-NOR gate using transmission gate technology. Explain its operation.

d) What do you understand by short channel effects? Explain.

e) Consider a CMOS inverter, with the following device parameters,

$V_{To,n}$= 0.8 V, μ_n. C_{ox} = 50 μA/V^2, $V_{To,p}$ = -1.0 V, μ_p. C_{ox} = 20 μA/V^2

Power supply is 5 V. Both transistors have equal channel length $L_n = L_p$ = 1 μm. Total Output load capacitance is C_{out} = 2 pF which is independent of transistor dimensions.

(i) Determine the channel width of the nMOS and the pMOS transistors such that the switching threshold voltage is equal to 2.2 V and the rise time is 5 ns.

(ii) Calculate the average propagation delay for the circuit designed in the first part.

f) Draw the CMOS based circuit diagram for the function F = A'B +C'(A'+B).

g) What is a ring oscillator? Explain with proper diagram. Mention the advantages and limitation of ring oscillators.

h) Design a 6 to 1 multiplexer using pass transistor logic.

i) What do you understand by precharge and evaluation in context of dynamic circuits. If a domino gate is at '1' at the start of evaluation can it make any other transition during evaluation. Why or why not? Explain briefly.

j) Draw a layout diagram for a two input Ex-OR gate using CMOS logic. Explain your diagram.

k) What are domino CMOS logic circuits.Discuss about charge sharing problems in these circuits.

l) Compare between FPGA and ASIC design approaches.

Part-III

Long Answer Type Questions (Answer Any TWO out of FOUR)

Q3 Find the values of high noise margin(NM_H) and low noise margin(NM_L) for a CMOS inverter with proper derivation. **(16)**

Q4 With the help of clear diagrams explain the fabrication steps for a n-well based CMOS inverter. **(16)**

Q5 **Write a note on :**

a) Current monitoring IDDQ technique. **(8)**

b) Built in Self test. **(8)**

Q6 **Write a note on :**

a) VLSI design rules. **(8)**

b) CAD tools. **(8)**