Registration No : | | | | | | | | | | |

Total Number of Pages : 01 **B.Tech**
PCS5I001

5th Semester Regular / Back Examination 2018-19
ADVANCED COMPUTER ARCHITECTURE
BRANCH : CSE
Time : 3 Hours
Max Marks: 100
Q.CODE : E488

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 **Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) Justify how RISC supports pipelining.
b) Show the relationship of CPI with the performance of a computer.
c) What is the importance of MFLOP over MIPS in computer designing.
d) What are the addressing modes used in JUMP and ADD R1,R2,R3 ?
e) State the difference between big- and little-endian representation.
f) Derive the expression of throughput of a pipelined computer.
g) Differentiate between WAW and WAR hazard with examples of each.
h) Enlist the factors affecting “Cache miss” while memory designing.
i) Provide one example of structural hazard caused due to memory accesses.
j) Map NUMA and UMA concepts of computers to Flynn’s classification with their justification.

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Explain Tomasulo’s approach for solving data hazard.
b) Differentiate between Synchronous and Asynchronous Pipelining.
c) State the difference between RISC and CISC computers.
d) Suppose that we are considering an enhancement that runs 10times faster than the original machine but is only usable 40% of the time. What is the overall speed up gained by incorporating the design?
e) Describe Flynn’s classification with their figure.
f) Give 3 examples of page replacement techniques with example.
g) Discuss one technique to incorporate instruction level parallelism with an example.
h) Describe different Pipeline hazards with their examples.
i) Explain two techniques to overcome RAW hazard.
j) Write 6 network topologies with their advantages.
k) Compare static and dynamic topologies.
l) What is the difference between superscalar and super pipelined processor.

Part-III

Long Answer Type Questions (Answer Any Two out of Four)

Q3 Write 6 cache optimization techniques. **(16)**

Q4 Suppose that in 1000 memory references there are 40 misses in the first level of cache and 20 misses in the 2nd level of cache. Assuming the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle and there are 1.5 memory references per instruction, calculate average memory access time **(16)**

Q5 Write the use of virtual memory and then justify paged segmentation scheme. **(16)**

Q6 Describe the techniques to overcome the cache coherence problem **(16)**