Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**
PCS3I101

3rd Semester Regular / Back Examination 2018-19
SWITCHING THEORY & LOGIC DESIGN
BRANCH : CSE
Time : 3 Hours
Max Marks : 100
Q.CODE : E723

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.
The figures in the right hand margin indicate marks.

Part- I

Q1 **Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) Determine the base of the numbers in each case for the following operations to be correct:
(i) 14/2 = 5 (ii) 24 + 17 = 40.
b) Show that the dual of the exclusive-OR is equal to its complement.
c) Differentiate between AND-OR-INVERT and OR-AND-INVERT.
d) What do you mean by universal gates?
e) Differentiate between error-detecting and error-correcting codes.
f) What do you mean by don't care conditions? Why it is used?
g) Define race around condition.
h) What is hazard? What is the impact of static 0 and static 1 hazards?
i) State De Morgan's theorem.
j) What do you mean by priority encoder?

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) The state of a 12-bit register is 100010010111. What is its content if it represents
(i) Three decimal digits in BCD?
(ii) Three decimal digits in the excess-3 code?
(iii) Three decimal digits in the 84-2-1 code?
(iv) A decimal number?
b) Obtain the truth table of the following functions and express each function in sum-of-min-terms and product-of-maxterms form:
(i) (b + cd)(c + bd)
(ii) (cd + b'c + bd') (b + d)
c) Draw a NAND logic diagram that implements the complement of the following function:
F(A, B, C, D) = Σ(0, 1, 2, 3, 6, 10, 11, 14)
d) Simplify the following Boolean functions, using four-variable maps:
(i) F(w, x, y, z) = Σ(1, 4, 5, 6, 12, 14, 15)
(ii) F(A, B, C, D) = Σ(0, 2, 4, 5, 6, 7, 8, 10, 13, 15)
e) Design a combinational circuit with three inputs and one output.
(i) The output is 1 when the binary value of the inputs is less than 3. The output is 0 otherwise.
(ii) The output is 1 when the binary value of the inputs is an even number.
f) Construct a JK flip-flop using a D flip-flop, a two-to-one-line multiplexer and an inverter.
g) What is the difference between serial and parallel transfer? Explain how to convert serial data to parallel and parallel data to serial. What type of register is needed?

h) The contents of a four-bit register is initially 0110. The register is shifted six times to the right with the serial input being 1011100. What is the content of the register after each shift?

i) A binary ripple counter uses flip-flops that trigger on the positive-edge of the clock. What will be the count if
(i) the normal outputs of the flip-flops are connected to the clock and
(ii) the complement outputs of the flip-flops are connected to the clock?

j) Design a four-bit binary synchronous counter with D flip-flops.

k) Explain the salient features of the ASM chart.

l) Explain how the ASM and ASMD charts differ from a conventional flowchart?

Part-III

Long Answer Type Questions (Answer Any Two out of Four)

Q3 Explain adder, subtractor, multiplexers and demultiplexers with suitable diagrams, illustrations and implementations. **(16)**

Q4 Explain SR, D, JK and T flip-flops with logic diagrams and function tables. **(16)**

Q5 Give the block diagram and the circuit diagram of a four-bit universal shift register that has all the capabilities and Explain. Give the state table of a BCD counter and Explain. **(16)**

Q6 Explain sequential binary multiplier with a block diagram. Show the register configuration of the data path. Give a numerical example for binary multiplier. **(16)**