Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech**

PET3I104

3rd Semester Regular / Back Examination 2018-19

DIGITAL ELECTRONICS

BRANCH : ECE, ETC

Time : 3 Hours

Max Marks : 100

Q.CODE : E891

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

Q1 **Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) An 8-bit 2's complement numeral system can represent integers in the range_____to_____.

b) $(24)_b + (17)_b = (40)_b$. Determine b.

c) -46-25. Perform the operation using 2's complement method.

d) Implement X-NOR using NOR gates only.

e) Find the total propagation delay time of a conventional 4-bit adder and a 4-bit adder with carry look ahead with the given data.
Propagation delay of exclusive-OR, AND and OR gate is 10ns, 5ns and 5ns respectively.

f) Design Y=AB using multiplexer.

g) How error can be detected and corrected in received binary bits?

h) Differentiate between asynchronous and asynchronous sequential circuits.

i) What do you mean by figure of merit of a logicc family?

j) Write the VHDL code for the Boolean expression of a 2-input NAND gate. Assume the delay of gate is 6ns.

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) Simplify the following expression in POS. Implement using NOR only.
$F(A, B, C, D) = \pi(0, 1, 2, 3, 4, 10, 11)$

b) Simplify the following Boolean function F, together with the don't care condition'd'. Implement the simplified expression using NAND only.
$F(A, B, C, D) = \sum(0,6,8,13,14)$
$d(A,B,C,D) = \sum(2,4,10)$

c) Implement a two bit magnitude comparator circuit using 2to4 size decoders.

d) Explain the operation of Full-subtractor circuit. Derive and Implement a Full-subtractor circuit using Half-subtractor.

e) Implement the following function with the help of 4:1multiplexers.
$F=\Sigma(1,2,3,5,11,12,15)$

f) The content of a 4-bit shift register is initially 1101. The register is shifted six times to the right with the serial input being 110101. Show the content of the register after each shift.

g) Design a MOD-12 counter using MOD-4 and Mod-3 counter. Explain the operation.

h) The three stage Johnson counter with initial state of $Q_2Q_1Q_0 = 101$ as shown in figure-1 is clocked at a constant frequency of 'f_c'. If the circuit is triggered for six pulses, then draw the corresponding output waveforms of Q_2, Q_1 and Q_0 in each pulse.

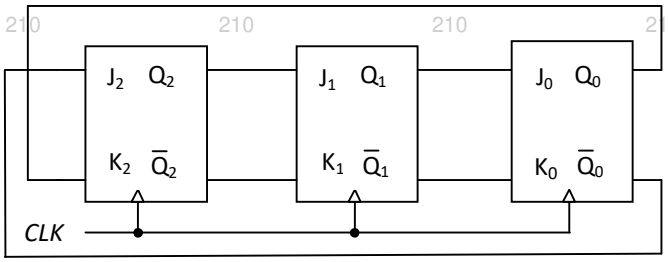

Figure-1

i) Describe the performance parameters considered in digital integrated circuits.

j) Using VHDL, design a binary UP counter that counts 0 to 7.

k) With neat circuit diagram, explain a RAM consisting of 4 words of 3bits each.

l) With neat diagram, explain TTL inverter.

Part-III

Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** Explain the rules of 1's complement addition and subtraction with suitable example. **(8)**

b) Design a 2-bit BCD adder circuit. **(8)**

Q4 **a)** Design a four-bit combinational circuit 2's complementer. Show that the circuit can be constructed with exclusive-Or gates. **(8)**

b) Assuming two numbers of 4-bit each, mention the overflow rules in addition and subtraction operation. Hence, design and explain a 4-bit adder-subtractor circuit. **(8)**

Q5 **a)** What is race-around condition? How does it get eliminated in a Master-slave configuration? Explain with neat diagrams. **(8)**

b) Design a 4-bit synchronous counter using J-K flip-flops. Use K-maps. **(8)**

Q6 **a)** Explain in brief the three modeling styles in VHDL. **(8)**

b) Explain the working of basic TTL NAND gate with a neat diagram. Describe Open collector and Totem-pole output. **(8)**