Registration No :

Total Number of Pages : 02 **B.Tech**

15BE2101

1st Semester Back Examination 2018-19

BASICS OF ELECTRONICS

BRANCH : AEIE, AERO, AUTO, BIOMED, BIOTECH, CHEM, CIVIL, CSE, ECE, EEE, EIE, ELECTRICAL, ENV, ETC, FASHION, FAT, IEE, IT, ITE, MANUFAC, MANUTECH, MARINE, MECH, METTA, METTAMIN, MINERAL, MINING, MME, PE, PLASTIC, TEXTILE

Time : 3 Hours

Max Marks : 100

Q.CODE : E949

Answer Question No.1 (Part-1) which is compulsory, any EIGHT from Part-II and any TWO from Part-III.

The figures in the right hand margin indicate marks.

Part- I

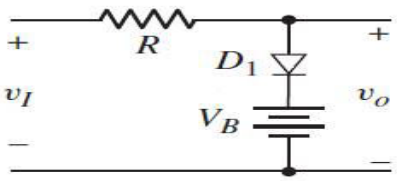
Q1 **Short Answer Type Questions (Answer All-10)** **(2 x 10)**

a) What is the slew rate of OP-AMP? What is its importance?
b) Is JFET is more advantageous than the BJT? Justify
c) Convert decimal number 151.75 to binary.
d) Calculate I_c , I_e and β_{dc} for a transistor that has α_{dc}=0.98 and I_B= 100μA
e) Define virtual ground concept of an op-amp.
f) Differentiate between enhancement type MOSFET and depletion type MOSFET and write down shockley's equation
g) Perform $(15)_{10}$-$(5)_{10}$ in binary.
h) What is ripple factor ? Mention its value for full-Wave rectifier.
i) Implement AND gate using NOR gates.
j) Draw a binary adder using logic gates.

Part- II

Q2 **Focused-Short Answer Type Questions- (Answer Any Eight out of Twelve)** **(6 x 8)**

a) What is a DC load line? Explain with a fixed bias circuit diagram. Also explain the importance of the Q-point or operating point.
b) Drawthe waveform V_o for V_i= 10 Sinωt, V_B=2V and $D_i$as silicon diode.



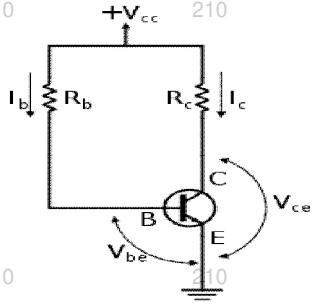
c) Design an integrator circuit using OP-AMP.
d) Draw the circuit diagram of the bridge type full-wave rectifier and explain how it works?
e) Distinguish between Zener breakdown and Avalanche breakdown
f) Convert the Boolean function in sum of products(SOP) form and minimize it.
F(A,B,C,D)=Σ(2,3,8,10,11,12,14,15)
g) With the help of a diagram, describe the basic structure an n- channel MOSFET. Give the biasing arrangement.
h) Explain BJT as an amplifier with example.
i) Write short note on CMOS.
j) Determine the diode current at 20^0C for a silicon diode with a reverse saturation current of 50nA and an applied forward bias voltage of 0.6 V.
k) What is a clamper circuit? Explain a positive clamper circuit with neat diagram.
l) With a neat diagram explain a voltage-Divider DC biasing circuit.

Part-III

Long Answer Type Questions (Answer Any Two out of Four)

Q3 **a)** Define I_{CBO}, I_{CEO}. Derive an expression to find the relation between them. **(8)**

b) Determine the values of I_C, V_{CC}, R_B and β for the biasing c circuit in Fig. where R_C=2.2kΩ, V_{CE} = 7.2 V, I_e=4mA, I_b= 20μA. **(8)**



Q4 **a)** With neat diagram, explain Input and Output characteristics of common emitter configuration. **(8)**

b) Using NAND logic gates derive all the other logic gates. **(8)**

Q5 **a)** Find out the expression for the rms voltage, dc voltage, and peak inverse voltage (PIV) for the full wave center-tapped rectifier **(8)**

b) Briefly discuss the operation of a n channel JFET and its output characteristic. **(8)**

Q6 **a)** Write properties of Ideal OP-AMP. Explain the output of a inverting OP-AMP circuit with neat diagram. **(8)**

b) Draw the output waveform for the given circuit with explanation.