Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech.**

PEI4I103

4th Semester Regular / Back Examination 2017-18

DIGITAL ELECTRONICS

BRANCH : AEIE, EIE, IEE

Time : 3 Hours

Max Marks : 100

Q.CODE : C895

Answer Part-A which is compulsory and any four from Part-B.
The figures in the right hand margin indicate marks.
Answer all parts of a question at a place.

Part – A (Answer all the questions)

Q1 **Answer the following questions: *multiple type or dash fill up type*** **(2 x 10)**

a) 1's complement of 101010_2 is _____.
b) Hexadecimal equivalent of 1110_2 is _____
c) Expansion of SOP is _____
d) Expand PLA _____
e) Number of digits a flip-flop can store is _____
f) The output of AND gate will be 1 only when all of its inputs are equal to _____
g) PAL contains programmable _____ gates.
h) PISO register means _____
i) Fastest IC logic family is _____
j) Fastest ADC technique is _____

Q2 **Answer the following questions: *Short answer type*** **(2 x 10)**

a) Subtract 101011_2 from 111001_2 using 2's complement method.
b) What are universal logic gates and draw their logic symbols.
c) Define the terms: minterm and maxterm
d) What are the applications multiplexing?
e) What are the applications of D-flip-flop?
f) Compare sequential and combinational logic circuits.
g) What is the difference between Mealy and Moore models?
h) Differentiate between synchronous and asynchronous counters.
i) Why ECL is the fastest among all other logic families?
j) List out various Digital to analog conversion techniques available.

Part – B (Answer any four questions)

Q3 **a)** Convert the following binary numbers to decimal and Hexadecimal numbers. **(10)**
(i) $(101101.1101)_2$ (ii) $(1101101.01)_2$
b) Solve the given expression using consensus theorem. **(5)**
A'B'+AC+BC'+B'C+AB

Q4 **a)** Reduce the following function using Karnaugh map method. **(10)**
$F(A,B,C,D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 4)$
b) Convert the given expression in standard SOP form. **(5)**
Y = AC + AB + BC

Q5	**a)**	Draw the logic circuit of 3-to-8 decoder and explain.	**(10)**
	b)	Draw the logic diagram of 2 bit binary adder along with the truth table.	**(5)**
Q6	**a)**	Implement the following function using 8:1 mux. $F(A,B,C,D) = \sum m(0, 1, 3, 4, 8, 9, 15)$	**(10)**
	b)	What are encoders?	**(5)**
Q7	**a)**	With a neat logic diagram explain how T flip-flop can be converted to D-Flip-flop.	**(10)**
	b)	What are the applications of SR flip-flop?	**(5)**
Q8	**a)**	With a neat circuit diagram explain the operation of RTL implementation of 2-input NOR gate.	**(10)**
	b)	What are the differences between RAM and ROM?	**(5)**
Q9	**a)**	With a neat diagram explain the operation of successive operation ADC.	**(10)**
	b)	Compare all the ADC's available.	**(5)**