Registration no: | | | | | | | | | | |

Total Number of Pages: 03 **B.TECH**

PEL4I103

4th Semester Regular / Back Examination 2017-18
DIGITAL ELECTRONICS CIRCUIT
BRANCH(S): EEE
Time: 3 Hours
Max marks: 100
Q.CODE:C774

Answer Question No.1 & Question No.2 which are compulsory and any four from the rest.

The figures in the right hand margin indicate marks.

Answer all parts of a question at a place.

Q1 Answer the following questions: **(2 x 10)**

a) The NAND gate output will be low if the two inputs are
(A) 00 (B) 01 (C)10 (D) 11

b) A ring counter consisting of five Flip-Flops will have
(A) 5 state (B) 2^5 states (C) $(2)^{25}$ states (D) Infinite states.

c) If the input to T-flipflop is 100 Hz signal, the final output of the three T-flipflops in cascade is
(A) 1000 Hz (B) 500 Hz (C)333 Hz (D) 12.5 Hz.

d) $(734)_8$ = (_____)$_{16}$
(A) C 1 D (B) D C 1 (C) 1 C D (D) 1 D C

e) If J = K (J and K are shorted) in a JK flip-flop, what circuit is made
A. SR flip-flop
B. Shorted JK flip-flop
C. T flip-flop
D. K flip-flop

f) A device which converts BCD to Seven Segment is called _____
(A) Encoder (B) Decoder (C) Multiplexer (D) Demultiplexer

g) The hexadecimal number 'A0' has the decimal value equivalent to_____

h) How many Flip-Flops are required for mod-16 counter?
(A) 5 (B) 6 (C) 3 (D) 4

i) The Boolean expression A.B' + A'.B + A.B is equivalent to_____

j) The minimal function that can detect a "divisible by 3" 8421 BCD code digit (representation is D_8 D_4 D_2 D_1) is given by
A. $D_8D_1+D_4D_2+D'_8D_2D_1$
B. $D_8D_1+D_4D_2\ D'_1+\ D'_4D_2\ D_1+D'_8\ D'_4D'_2D'_1$
C. $D_8D_1+D_4D_2+\ D'_8\ D'_4D'_2D'_1$
D. $D_4D_2\ D'_1+\ D_4D_2\ D_1+\ D_8\ D'_4D_2D_1$

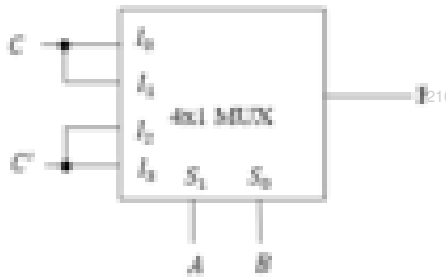
Q2 Answer the following questions: **(2 x 10)**

a) 2's complement representation of a 16 bit number (one sign bit and 15 magnitude bits) is FFFF. Represent its magnitude in decimal.

b) What is race around condition? How to over come to this situation.

c) Draw the flip-flop output waveforms of a 4-bit SISO shift register assuming the initial data stored in the register is 1001?

d) What is the expression for the Boolean Function F in the circuit shown in the figure below?



e) If (AB)' + A'B= C then find (AC)' + A'C

f) What is priority encoder? Write the truth table of 4 input priority encoder.

g) State the difference between edge triggering and level triggering.

h) How many numbers of Boolean functions that can be generated by n variables?

i) Compare the characteristics equation of R-S Flip-Flop with J-K Flip-Flop.

j) Realize the Boolean expression Y= (x+y)(x+y') using NAND gates.

Q3 **a)** Design a comparator circuit that compares two '4' bit Numbers A and B With all conditions. **(10)**

b) Find the dual and complement of the following Boolean expression F(x,y,z) = x'yz+x'yz'+xy'z'+xy'z **(5)**

Q4 **a)** Implement the Boolean Function $F(A,B,C,D) = \sum(1,3,4,11,13,14,15)$ using 4X1 MUX? **(10)**

b) Construct a 5-to 32-line decoder with four Nos of 3-to 8-line decoder having enable line and a 2- to 4-line decoder. Use block diagram for the components? **(5)**

Q5 **a)** A PN flip-flop has four operations: clear to '0', no change, complement and set to '1', when inputs P and N are 00,01,10,11 respectively. Tabulate the characteristic table and derive the characteristic equation? **(8)**

b) Design a mod 4 synchronous counter using J-K Flip Flop and implement it. **(7)**

Q6 **a)** With neat sketch, explain the operation of a 3-bit universal shift register **(8)**

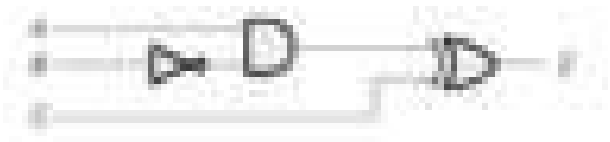
b) Design a 3 x 8 decoder and Implement it using a suitable PLA. **(7)**

Q7 **a)** The K - map for a Boolean function is shown in the figure below. Find out the number of essential prime implicants for this function? **(10)**

AB / CD	00	01	11	10
00	1	1	0	1
01	0	0	0	1
11	1	0	0	0
10	1	0	0	1

b) With proper block diagram explain SAR type ADC (Analog to Digital Converter) **(5)**

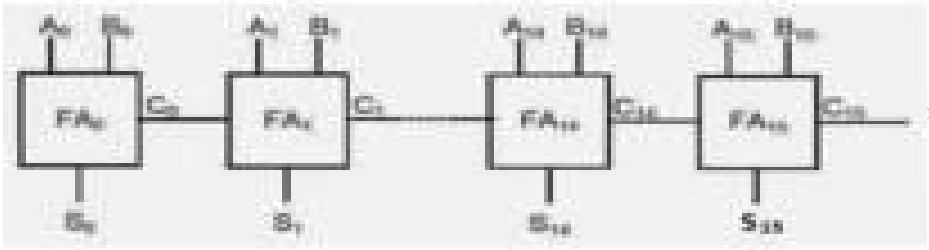
Q8 **a)** All the logic gates shown in the figure have a propagation delay of 20 ns. Let A=C=0 and B=1 until time t=0. At t=0, all the inputs flip (i.e. A=C=1 and B=0) and remain in that state. For t>o. for how much duration (in ns) the output (z) will be at logic 1. Explain? **(10)**



b) Explain the operation of a 8 x 1 Multiplexer and Implement the following function using a suitable Multiplexer **(5)**

$F(A, B, C, D) = \sum m\ (0, 1, 3, 5, 6, 7, 8, 9, 11, 13, 14)$

Q9 **a)** A 16 bit ripple carry adder is realized using 16 identical full adders (FA) as shown in the figure. The "**carry"** propagation delay of each FA is 12 ns and the **"sum"** propagation delay of each FA is 15 ns. Find the worst case delay (in ns) of this 16 – bit adder? **(10)**



b) Design an EX-OR gate using CMOS only. **(5)**