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Total Number of Pages : 02

B.Tech.  
PCEC4202

4<sup>th</sup> Semester Back Examination 2017-18

DIGITAL ELECTRONIC CIRCUIT

BRANCH : AEIE, BIOMED, CSE,  
ECE, EEE, EIE, ELECTRICAL, ETC, IEE, IT, ITE

Time : 3 Hours

Max Marks : 70

Q.CODE : C667

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

Answer all parts of a question at a place.

**Q1** Answer the following questions : (2 x 10)

- Convert decimal number 214 to its octal equivalent.
- Draw the logic symbols and truth tables of universal logic gates.
- Solve the given expression using consensus theorem.  
 $A'B' + AC + BC' + B'C + AB$
- Define the terms: mInterm and maxterm.
- Define the terms: entity and attribute.
- Write the behavioral model of a simple AND gate.
- Differentiate between inertial and transport delays.
- What is VLSI and what are its advantages?
- Draw the logic symbols of Multiplexer and Demultiplexer.
- Write any four differences between RAM and ROM.

**Q2** a) Subtract  $101011_2$  from  $111001_2$  using 1's complement and 2's complement methods. (5)

b) Convert the given expression in standard POS form. (5)  
 $Y = A.(A+B+C)$

**Q3** a) Show the realization of all logic gates using universal logic gates. (5)

b) Reduce the following function using Karnaugh map method. (5)  
 $F(A,B,C,D) = \sum m(1, 3, 7, 11, 15) + \sum d(0, 2, 4)$

**Q4** a) Write the behavioral model of a 4X1 Mux. (5)

b) Explain various data types used in VHDL. (5)

**Q5** a) Draw the circuit diagram of CMOS inverter and explain its operation. (5)

b) What are the advantages with CMOS logic? (5)

**Q6** a) What are the differences between sequential and combinational networks? (5)

b) Draw the logic diagram of 2 bit binary adder and explain its operation. (5)

**Q7** Draw the logic diagram of master slave flip-flop and explain its operation. **(10)**

**Q8** Write short answer on any TWO : **(5 x 2)**

- a) Canonical logic forms
- b) MOSFET design rules.
- c) Flip-Flops
- d) State machines