Registration No : | | | | | | | | | | |

Total Number of Pages : 02 **B.Tech.**

PCS4I101

4th Semester Regular / Back Examination 2017-18

COMPUTER ORGANIZATION & ARCHITECTURE

BRANCH : CSE

Time : 3 Hours

Max Marks : 100

Q.CODE : C675

Answer Part-A which is compulsory and any four from Part-B.

The figures in the right hand margin indicate marks.

Answer all parts of a question at a place.

Part – A (Answer all the questions)

Q1 **Answer the following questions : *multiple type or dash fill up type :*** **(2 x 10)**

a) In case of Zero-address instruction method the operands are stored in _____
i) Registers ii) Accumulators iii) Push down stack iv) Cache

b) The data structure suitable for scheduling processes is _____
i) List ii) Heap iii) Queue iv) Stack

c) The decoded instruction is stored in _____
i) IR ii) PC iii) Registers iv) MDR

d) The instructions like MOV or ADD are called as _____
i) OP-Code ii) Operators iii) Commands iv) None of the mentioned

e) The program is divided into operable parts called as _____
i) Frames ii) Segments iii) Pages iv) Sheets

f) _____ addressing mode is most suitable to change the normal sequence of execution of instructions.
i) Relative ii) Indirect iii) Index with Offset iv) Immediate

g) The techniques which move the program blocks to or from the physical memory is called as _____
i) Paging ii) Virtual memory organization iii) Overlays iv) Framing

h) The DMA doesn't make use of the MMU for bulk data transfers.
i) True ii) False

i) In associative mapping during LRU, the counter of the new block is set to '0' and all the others are incremented by one,when _____ occurs.
i) Delay ii) Miss iii) Hit iv) Delayed hit

j) If, the sub routine exceeds the private space allocated to it then the values are pushed onto _____
i) Stack ii) System heap iii) Reserve Space iv) Stack frame

Q2 **Answer the following questions : *Short answer type :*** **(2 x 10)**

a) List out the disadvantages of DRAM over SRAM.

b) Perform the arithmetic operations 35 + 40 and (- 35) + (- 40) with binary numbers in singed 2's complement representation and signed magnitude representation.

c) Explain Cache Coherency problem.

d) Write the difference between micro processor and a micro program.

e) Mention what is a vector interrupt?

f) Distinguish between Memory Mapped I/O and I/O Mapped I/O.

g) Define strobe control.

h) Which techinque is used to automatically move program and data blocks into the physical memory when they are required for execution ?

i) Compare RISC and CISC instructions.

j) Differentiate between array processing and vector processing.

Part – B (Answer any four questions)

Q3 **a)** Design a neat labeled diagram of working principle of single bus organization of the data path inside the CPU. **(10)**

b) Explain the hardware implementation of logical micro operation for AND, OR, XOR and Compliment logic gates? **(5)**

Q4 **a)** Enlist the types of memory mapping techniques used in cache memory. **(10)**

b) An instruction is stored at location 300 with its address field at location 301. The address field has the value 400. A processor register R1 contains the no 200. Evaluate the Effective Address if the addressing mode of the instruction is : **(5)**

i) Direct
ii) Immediate
iii) Relative
iv) register Indirect
v) Index with R1 as the Index Register

Q5 **a)** Distinguish between hardwired controlled unit and micro programmed controlled unit. **(10)**

b) Design the memory hierarchy in a computer system. **(5)**

Q6 **a)** Explain the importance of different addressing modes in computer architecture with suitable example. **(10)**

b) How can you illustrate the performance of memory? **(5)**

Q7 **a)** Why does DMA have priority over the CPU when both request a memory transfer? **(10)**

b) Write short notes on RS-232C, IEEE-488, USB. **(5)**

Q8 **a)** What is the basic advantage of using interrupt initiated data transfer over transfer under program control without an interrupt? **(10)**

b) Design the hardware of addition & subtraction of fixed point signed magnitude numbers. **(5)**

Q9 **a)** Multiple (-7)10 with (3)10 by using Booth's multiplication. Give the flow table of the multiplication. **(10)**

b) Write short note on TLB. **(5)**