

Registration No:

--	--	--	--	--	--	--	--	--	--

Total Number of Pages : 02

B.Tech.
15BE2101

1st Semester Back Examination 2017-18

BASIC ELECTRONICS

BRANCH: AERO, CHEM, CIVIL, CSE, ECE, EEE, ELECTRICAL, ETC, IT, MECH, MME,
PE, PLASTIC, TEXTILE

Time: 3 Hours

Max Marks: 100

Q.CODE: B999

Answer Question No.1 and 2 which are compulsory and any four from the rest.
The figures in the right hand margin indicate marks.

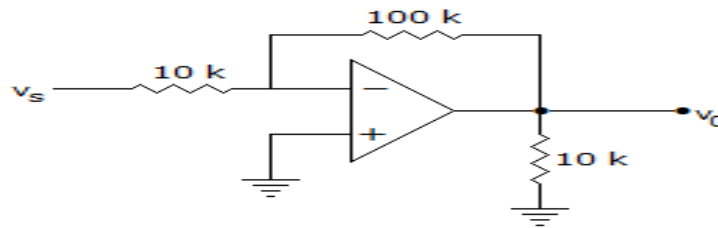
Q1 Answer the following questions: *multiple type or dash fill up type* (2 x 10)

- a) The thermal runaway in a CE transistor amplifier can be prevented by biasing the transistor in such a manner that
a) $V_{CE} > V_{CC}/2$ b) $V_{CE} < V_{CC}/2$ c) $V_{CE} = V_{CC}/2$ d) $V_{CE} = 0$
- b) A diode is said to be useful to be configured as an amplifier when its β is
a) Less than 0 b) between 0 & 1
c) between 1 & 50 d) > 50
- c) A full wave rectifier needs at least ----- diodes.
- d) The maximum efficiency of an half wave rectifier is ----- %.
- e) The frequency compensation is used in Op-Amps to increase its -----.
- f) An Instrumentation amplifier uses ----- Op-Amps.
- g) Which of the following is not associated with a p-n junction
a) junction capacitance
b) charge storage capacitance
c) depletion capacitance
d) channel length modulation
- h) 9's complement of 68 is -----
The decimal equivalent of 10010111 is -----
- i) What is mean by PIV rating of a diode
a) Maximum reverse bias potential which can be applied across a diode without breakdown
b) Maximum forward bias potential which can be applied across a diode without breakdown
c) Minimum potential required by a diode to reach conduction state
d) Maximum power allowable to a diode
- j) SR Flip flop can be converted to T-type flip-flop if

Q2 Answer the following questions: *Short answer type* (2 x 10)

- a) Define CMRR and Slew rate.
- b) Difference between zener breakdown and avalanche breakdown.
- c) Derive the relation between α and β .
- d) Prove Demorgan's Theorem.
- e) Draw the IEEE logic symbol of AND, NOT, NOR & XOR gates.
- f) Define Bark Hausen criterion.
- g) Give the relationship between I_{CO} & I_{CEO} .
- h) Define the thermal runaway of transistor.
- i) What is common collector configuration of BJT ?

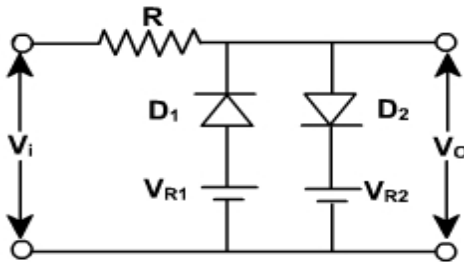
j)



What is input impedance of op-amp circuit in the above figure?

Q3 a) With neat circuit diagram and waveforms, explain the working of a full wave bridge rectifier. Also discuss the PIV for center tapped Transformer. **(10)**

b) **(5)**



Discuss the above circuit with sinusoidal input of peak to peak voltage 10 V, $V_{R1} = 2V$, $V_{R2} = 1V$, $R = 1\Omega$, and the diodes are silicon diodes

Q4 a) The i/p to the Full wave rectifier is $v(t) = 200 \sin 50t$. If R_L is $1k\Omega$ and forward resistance of diode is 50Ω , find: **(10)**

- D.C current through the circuit
- The A.C (rms) value of current through the circuit
- The D.C output voltage
- The A.C power input
- The D.C power output
- Rectifier efficiency.

b) Explain zener diode voltage regulator circuit with no load and with load. **(5)**

Q5 a) With a neat circuit diagram, explain the Voltage Divider Bias circuit using approximate analysis. Also derive the equation of stability (S) for Voltage Divider Bias circuit. **(10)**

b) What is a DC load line? Explain Base biased method with necessary equations. **(5)**

Q6 a) Design a single stage common source amplifier for following specification. $A_v = -25$, $V_0 = 2.5V$ **(10)**

b) Derive the expression of 3 input summing amplifier. **(5)**

Q7 a) Convert $(1101101)_2 = ()_{10}$ and $(69)_{10} = ()_2$ **(10)**
Convert $(101011101110101)_2 = ()_{16}$ and $(FA876)_{16} = ()_2$

b) Write notes on Universal Gates. Also realize NOR using NAND gates only. **(5)**

Q8 a) Factorize the following Boolean equations **(10)**

$$Y_1 = AB' + AB$$

$$Y_2 = (B + CA) + (C + A'B)$$

Write a note on Full Adder.

b) What is a RS Flip-Flop? Explain using its circuit diagram, logic symbol and truth table. **(5)**

Q9 a) Write the principle and working of CRO with proper block diagram. **(10)**

b) Write notes on **(5)**

- Virtual ground
- Clamper circuit