Registration No: | | | | | | | | | | |

Total Number of Pages: 03 **B.Tech.**
PCS3I101

3rd Semester Regular/Back Examination 2017-18
SWITCHING THEORY AND LOGIC DESIGN
BRANCH : CSE
Time : 3 Hours
Max Marks : 100
Q.CODE : B889

Answer Question No.1 and 2 which are compulsory and any four from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions: *multiple type or dash fill up type*** **(2 x 10)**

a) How many inputs of a four-input AND gate must be HIGH in order for the output of the logic gate to go HIGH?
A.any one of the inputs
B.any two of the inputs
C.any three of the inputs
D.all four inputs

b) One of De Morgan's theorems states that Simply stated, this means that logically there is no difference between:
A.a NOR and an AND gate with inverted inputs
B.a NAND and an OR gate with inverted inputs
C.an AND and a NOR gate with inverted inputs
D. a NOR and a NAND gate with inverted inputs

c) How many gates would be required to implement the following Boolean expression before simplification? XY + X(X + Z) + Y(X + Z)
A.1
B.2
C.4
D.5

d) Before an SOP implementation, the expression would require a total of how many gates?
A.1
B.2
C.4
D.5

e) On the fifth clock pulse, a 4-bit Johnson sequence is Q0 = 0, Q1 = 1, Q2 = 1, and Q3 = 1. On the sixth clock pulse, the sequence is _____.
A.Q0 = 1, Q1 = 0, Q2 = 0, Q3 = 0
B.Q0 = 1, Q1 = 1, Q2 = 1, Q3 = 0
C.Q0 = 0, Q1 = 0, Q2 = 1, Q3 = 1
D.Q0 = 0, Q1 = 0, Q2 = 0, Q3 = 1

f) Determine the output frequency for a frequency division circuit that contains 12 flip-flops with an input clock frequency of 20.48 MHz.
A.10.24 kHz
B.5 kHz
C.30.24 kHz
D.15 kHz

g) A MOD-16 ripple counter is holding the count 10012. What will the count be after 31 clock pulses?
A.10002
B.10102
C.10112
D.11012

h) If two inputs are active on a priority encoder, which will be coded on the output?
A.the higher value
B.the lower value
C.neither of the inputs
D.both of the inputs

i) How many 74184 BCD-to-binary converters would be required to convert two complete BCD digits to a binary number?
A.8
B.4
C.2
D.1

j) A carry look ahead adder is frequently used for addition, because it
A. Is faster
B. is more accurate
C. uses fewer gate
D. cost less

Q2 **Answer the following questions: *Short answer type*** **(2 x 10)**

a) What are the universal gates? Why they are called universal gate?
b) What are the differences of flip-flop and Latch?
c) Convert the following.
97710 = ( )16
d) How a D-flip flop obtained from JK flip flop? Write its truth table.
e) Convert the given expression in canonical SOP form y=AC+AB+BC.
f) What is edge-triggered flip-flop?
g) What is race around condition?
h) What are the applications of shift registers?
i) What is the basic type of counter made by flip-flop or resistor?
j) Distinguish between static and dynamic hazards.

Q3 **a)** Minimize the following function using K-map and also verify through tabulation method. **(10)**
F (A, B, C, D) = ∑m(1,4,5,7,8,9,12,14)+d (0, 3, 6, 10).

b) Reduce the following Boolean expression using Demorgan's theorems. **(5)**
AB+A (B+C) +B$^{|}$ (B+D)

Q4 **a)** Design BCD to gray code converter and realize using logic gates. **(10)**
b) Why a multiplexer is called a data selector? Draw the 2x1 MUX. **(5)**

Q5 **a)** Given the 8bit data word 01011011, generate the 12 bit composite word for the hamming code that corrects and detects single errors. **(10)**
b) Design half adder from 2 to 4 decoder **(5)**

Q6	**a)**	Explain the operation of 5-stage twisted ring counter with circuit diagram, state transition diagram and state table.	**(10)**
	b)	Draw the circuit of J – K master slave flip-flop with active high clear and active low preset.	**(5)**
Q7	**a)**	Define an encoder. Design octal to binary encoder.	**(10)**
	b)	Differentiate between an ASM chart and a conventional flow chart?	**(5)**
Q8	**a)**	Draw the logic diagram of a SR latch using NOR gates. Explain its Operation usingexcitation table.	**(10)**
	b)	Write the difference between combinational circuit and sequential circuit	**(5)**
Q9	**a)**	What is a shift register? Draw the block diagram and timing diagram of a shift register that shows the serial transfer of information from register A to register B.	**(10)**
	b)	Implement the following functions using NAND gates. a) $F1= A (B+C D) + (B C)^{I}$	**(5)**