Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**

PEEI5404

8th Semester Regular / Back Examination 2016-17

ANALOG VLSI DESIGN

BRANCH(S):ECE, ETC

Time: 3 Hours

Max Marks: 70

Q.CODE: Z265

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) What is the need for Amplification in Analog Circuit design?

b) What do you mean by **Common Source** in Common Source Amplifier?

c) Write the expression of the output of a Common Source Stage when the transistor goes into the deep triode region. Also give the gain of such an arrangement.

d) Draw the circuit configuration of a CS stage with current- source load? Where do this circuit fin their applications?

e) What type of circuit can you see in Figure Q1 (e)?

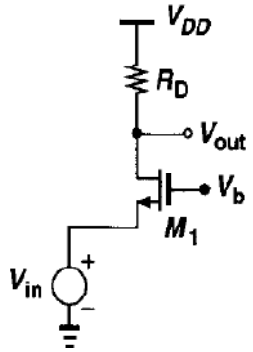

Figure Q1 (e)

f) How important is common mode to differential conversion?

g) What is a Variable Gain Amplifier? Mention its use.

h) Differential between a transimpedence and a transconductance amplifier.

i) What is a "diode connected" device? Draw the small signal equivalent circuit for a diode connected NMOS device.

j) Mention some drawbacks of a simple one stage OPAMP topology.

Q2 **a)** For a CS stage with source degeneration derive the voltage gain, equivalent transconductance of the circuit under both large and small signal conditions. **(8)**

b) Does the output resistance increase or decrease due to use of source degeneration for (a)? **(2)**

Q3 **a)** Define a VCO with proper illustrations. **(3)**

b) A VCO senses a small sinusoidal control voltage $V_{cont} = V_m \cos\omega_m t$. Determine the output waveform and its spectrum. **(7)**

Q4 Discuss different Feedback topologies. **(10)**

Q5 **a)** For the given circuit in Figure Q5 (a)calculate the transfer function with λ=0 and explain why Miller effect vanishes as C_{DB} increases **(5)**

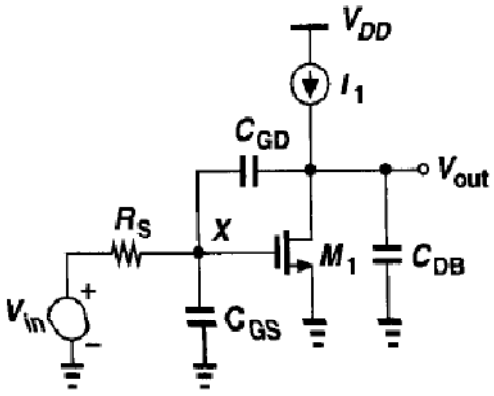

Figure Q5 (a)

b) Compute the transfer function of the common gate stage with parasitic capacitance in the following circuit in Figure Q5 (b). Neglect channel length modulation. **(5)**

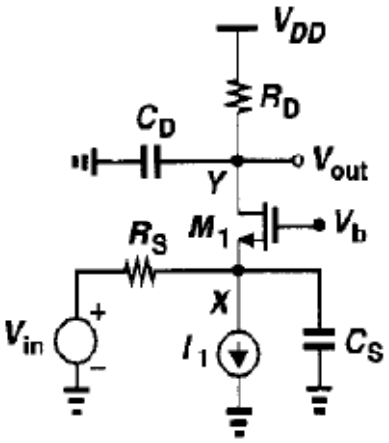

Figure Q5 (b)

Q6 **a)** Mention some useful properties of differential signalling. Give a modification that can resolve the issues faced by the simple differential circuit shown in Figure Q6 (a). **(5)**

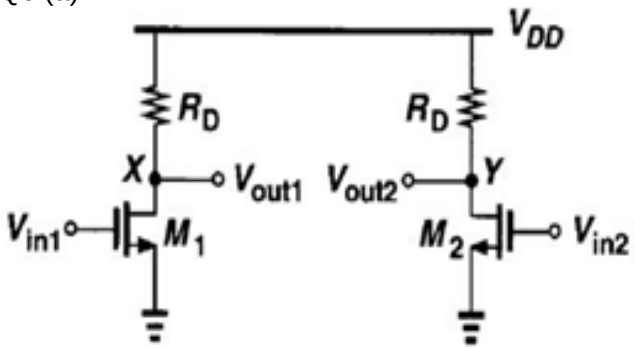

Figure Q6 (a)

b) Discuss the Differential pair operation with MOS loads. **(5)**

Q7 What is a Source Follower? Discuss about its input output characteristics and also derive its small signal gain. **(10)**

Q8 **Write short answer on any TWO:** **(5 x 2)**

a) Active Current Mirrors
b) CS Stage with Source Degeneration
c) Temperature-Independent References
d) Slew Rate and Power Supply Rejection in OPAMP