Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **B.Tech**
PEEI5404

8th Semester Regular / Back Examination 2016-17
ANALOG VLSI DESIGN
BRANCH(S):CSE, IT, ITE
Time: 3 Hours
Max Marks: 70
Q.CODE:Z398
Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 **Answer the following questions:** **(2 x 10)**

a) With the aid of a diagram show the various Levels of Abstraction.
b) Draw the circuit of the Common Source Stage with its small signal equivalent.
c) How can the gain of a Common Source stage be maximized?
d) Draw the circuit configuration and the input output characteristics of a Common Source stage with a diode connected load.
e) Mention one advantage and one drawback of the CS Stage with Triode Load?
f) What is the shielding property?
g) What is a folded cascode?
h) Draw a basic differential pair. Mention some of its use.
i) What is a Gilbert Cell? Mention its use.
j) Draw a Common Gate stage at high frequency and mention one important property of the same.

Q2 **a)** Discuss the effect of Loading in two port networks. **(8)**
b) The output resistance increase due to use of source degeneration? Explain. **(2)**

Q3 **a)** Draw the equivalent circuit for the Colpitts Oscillator topology. Calculate the voltage gain of the same. **(3)**
b) What is a VCO? What are the important parameters of VCO? **(7)**

Q4 Calculate the input and output impedence of a Source Follower. **(10)**

Q5 **a)** Define PSRR. Calculate the PSRR for the given circuit in Figure Q5 (a). **(5)**

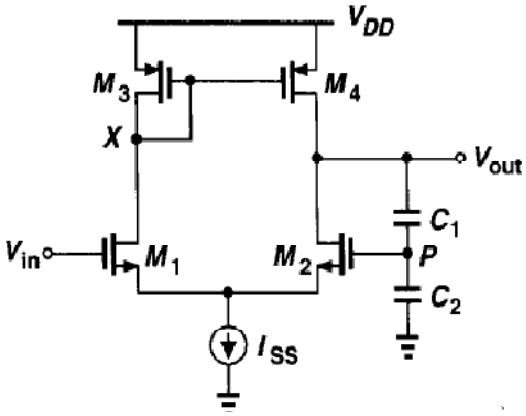

Figure Q5 (a)

b) Discuss the effect of Slewing in OPAMPs. **(5)**

Q6 **a)** Find the voltage gain of the common-source amplifier of Figure Q6 (a)with V_{DD}= 5V, R_D= 5kΩ, $k'=\mu_n C_{ox}$= 100μA/V^2,W= 50μm,L = 1μm,V_t= 0.8V,L_d = 0,X_d= 0,and λ = 0. Assume that the bias value of V_i is 1 V. **(5)**

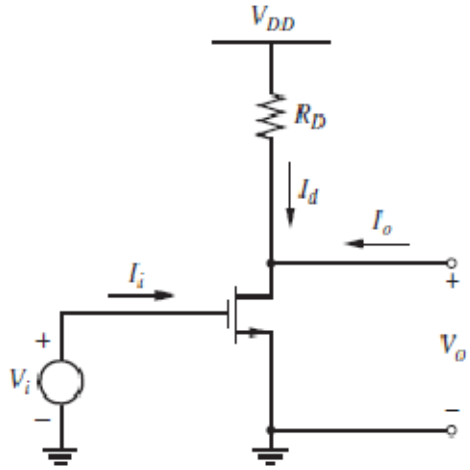

Figure Q6 (a)

b) For the given circuit in Figure Q6 (b), calculate the g_m and A_v. Also draw its small signal equivalent model. **(5)**

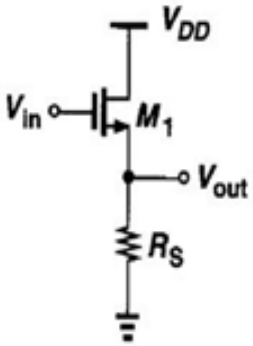

Figure Q6 (b)

Q7 What is the objective of Reference generation? What are the different design issues in Bandgap Reference? **(10)**

Q8 **Write short answer on any TWO:** **(5 x 2)**

a) Common-Source Stage with Resistive Load
b) Differential Pair with MOS Loads
c) Different types of Amplifier Configurations
d) LC Oscillator and Ring Oscillator