D17002118

**Registration No:** | | | | | | | | | | |

**Total Number of Pages : 02** **M.TECH**

**M.TECH 1ST SEMESTER REGULAR EXAMINATIONS, DECEMBER 2017**
**ADVANCED VLSI TECHNOLOGY**
**Branch: EC, Subject Code:MECPE1041**
**Time: 3 Hours**
**Max Marks : 70**
**The figures in the right hand margin indicate marks.**

## PART-A

**( 2X10=20 MARKS)**

**1. Answer the following questions .**

a) What is the need of clean room?

b) How a silicon wafer prepared? What is the crystal structure of silicon?

c) What is diffusion? Give one example?

d) What do you mean by annealing? Is it necessary?

e) Explain oxidation with one example?

f) What is photolithography?

g) Write down about photo resist materials?

h) What is the range of temperature required for oxidation and annealing?

i) What is RIE etching?

j) Why CMOS used for VLSI/ULSI circuit? Explain?

## PART-B

**(5 X 10=50 MARKS)**

**Answer any five questions from the following.**

2. a) Explain the n-well fabrication process of CMOS with neat diagram? **5**
   b) Write the VHDL code for a positive edge triggered D- type Flip-Flop. **5**

3. a) Phosphorus is diffused into a uniformly doped p-type silicon with $N_B = 10^{16}/cm^3$ at $1150^0C$.Given that the solid-solubility of phosphorus in silicon at $1150^0C$ is $10^{20}/cm^3$ and the diffusion coefficient at this temperature is $1*10^{-12}cm^2/sec$,(a)calculate the total number of phosphorus atoms per unit area of the silicon area of the silicon surface after a predisposition time of 1hour.(b)if after this, drive in is carried out for 2 hours at the same temperature, what will be the final junction depth and surface concentration? **7**
   b) Design a 2×1 multiplexer using CMOS transmission gate. **3**

4. a) Phosphorus is implanted in a p-type silicon sample with a uniform doping concentration of $10^{16}/cm^3$. If the beam current density is $2\mu A/cm^2$ and the implantation is carried out for ten minutes, calculate the implantation dose. Also find the peak impurity concentration assuming $R_P=1.1\mu m$ and $\Delta R_P=0.3\mu m$. **7**

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| b) What is E-Beam lithography? | | 3 |
| 5. a) Explain the CVD process with neat diagram? | | 5 |
| b) How mask has been generated for VLSI circuit? Design the layout of a NAND gate? | | 5 |
| 6. a) Differentiate plasma etching and RIE etching? | | 5 |
| b) Explain wafer cleaning process? | | 5 |
| 7. a) what is sputtering? Explain different sputtering techniques? | | 5 |
| b) Explain Annealing with neat diagram? | | 5 |
| 8. a) Explain about VLSI design methodology. | | 5 |
| b) Explain about the band diagram of a MOS system fabricated on a p-type substrate. | | 5 |

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