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Total Number of Pages : 01 M.TECH

M.TECH 1ST SEMESTER REGULAR EXAMINATIONS, DECEMBER 2017 PARALLEL COMPUTING

Branch: CS, Subject Code:MCSPE1042

Time: 3 Hours Max Marks: 70

The figures in the right hand margin indicate marks.

<u>PART-A</u> (2X10=20 MARKS)

1. Answer the following questions.

- a) How Can One Ensure Mutual Exclusion Without Locks?
- b) Name Some Network Architectures Prevalent In Machines Supporting The Message Passing Paradigm?
- c) What is Task-parallel Computation?
- d) What is task-latency and task-throughput?
- e) What is the Maximum Time Speed-up possible according to Amdahl's Law?
- f) What is Cache Coherence?
- g) What is a Hypercube Connection? What is the diameter of an N-node Hypercube?
- h) What is the memory consistency model supported by OpenMP?
- i) What is the impact of eliminating shared write from PRAM?
- j) What is Accelerated Cascading?

(5 X 10=50 MARKS) **PART-B** Answer any five questions from the following. 5 2. Explain PRAM Model with its components. a. Explain Hypercube Network with properties. 5 b. Explain Bernstein conditions for detection of parallelism. 3. a. 5 Explain the concept of multithreading and its use in parallel computer b. 5 architecture. 4. Flynn's classification is based on multiplicity of instruction stream and data a) 5 stream observed by CPU during program execution. Explain in detail. What is the PRAM model? Which PRAM model can be used to execute b) any other PRAM algorithm and how? Discuss the following with respect to a parallel virtual machine. Compiling and running of a PVM program. Creating and managing Dynamic process group. 5 5. 5 a) 5 b) Explain the concept of multithreading and its use in parallel computer 6. a) 8 architecture. Define multi-threading models 2 b) 7. Define array processing. a) 2 b) Why are array processors called as SIMD Array computers? With the help 8 of a Block diagram. Explain the architecture of an SIMD array processor. 8. Write Short notes on 5 PRAM. a. 5 b. Cloud computing.