Registration no:
Total Number of Pages: 02

M.TECH
CSPE 210

Second Semester Examination – ~~2013~~ 2014

EMBEDDED SYSTEM

Time: 3 Hours

Max marks: 70

Answer Question No.1 which is compulsory and any five from the rest.

The figures in the right hand margin indicate marks.

1. Answer the following briefly. [2×10]

a) What is design turnaround time and why should it be as small as possible?
b) What are the modes of operation of ARM?
c) What do you mean by *safety-critical*?
d) To multiply 18 by -1, if 18 is in source, how many cycles needed by ARM?
e) What is *hot swapping*?
f) What do you mean by full custom device and device class?
g) What do you mean by *spread spectrum frequency hopping*?
h) What do you mean by a valid schedule and a feasible schedule?
i) What is dynamic power dissipation of a circuit?
j) Why IrDA is called a *line-of-sight* communication?

2. a) What do you mean by design metric? What are the various design metrics that need to be considered in embedded system design? [6]

b) What are the various tools needed in the embedded system design cycle? Explain each. [4]

3. a) What will be the content of the stack after executing each of the ARM instruction –

STMFD SP! $\{R_0, R_1, R_5–R_{12}\}$ STMED SP! $\{R_5–R_{12}\}$

STMFA SP! $\{R_2–R_5, R_8–R_{12}\}$ STMEA SP! $\{R_0–R_{12}\}$ [6]

b) What is THUMB? How THUMB instructions are executed by ARM? Is it advantageous? [4]

4. a) What is table driven scheduler? For the following task set, perform EDF scheduling. [6]

Task	Execution time	Periodicity
T1	1	3
T2	2	5
T3	4	10
T4	3	15

b) What is IIC? Draw a neat timing diagram for IIC transfer with start and stop. [4]

5.

a) What is the concept of Particle Swarm Optimization? How can it be applied in hardware- software partitioning? [5]

b) Write down Kernighan-Lin partitioning algorithm. Give a complexity analysis of this algorithm. [5]

6. Justify your answer. [2.5×4]

a) Whether embedded systems are single functioned?

b) Whether modification of condition flags by arithmetic instructions is optional?

c) Can clock-gating reduce dynamic power?

d) Whether RMS is a static priority algorithm?

7. Distinguish and differentiate

a) RISC Vs. CISC

b) Sporadic task Vs. Aperiodic task

c) Bulk transfer Vs. Isochronous transfer

d) FPGA Vs. CPLD

8.

a) What is emulation? What are the features of emulation? [5]

b) What do you mean by sequence diagram? Draw a sequence diagram for elevator operations. [5]
