Registration no: | | | | | | | | | | |

Total Number of Pages: 02

M.TECH
CSPC102

M.Tech First Semester Regular/Back Examination – 2015
ADVANCED COMPUTER ARCHITECTURE
BRANCH(S): CSE
Time: 3 Hours
Max marks: 70
Q.CODE: T970

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions: (2 x 10)

a) What do you mean by Cache-coherence?
b) State Amdahl's law and explain.
c) For single instruction execution which one is better between Pipeline and Non-pipeline system? Justify.
d) What do you mean by Temporal locality of reference?
e) What is an Exception in a pipeline?
f) Differentiate between Address space and Memory space.
g) What do you mean by mesh connected system..
h) What do you mean by Overheads in a pipeline?
i) What is a Delayed branch? How does it improve the Performance?
j) What do you mean by Highly pipelined system?

Q2 a) Whether parallelism can be achieved in Uni-processor system? Justify. (5)

b) What is a Cache? (5)

Consider a Cache size of 2K words with 16 words per block. The main memory has a capacity of 256K word.

i. Calculate number of bits in tag field, block flied and word field for direct mapping.
ii. Calculate number of bits in tag field and word field for fully associative mapping.
iii. Calculate number of bits in tag field, set field and word field for set associative mapping if one set consists of 2 blocks.

Q3

a) What do you mean by Pipeline Hazard? How control hazard is detected and resolved? Explain with time-space diagram. (5)

b) Identify the data hazards while executing the following instruction in DLX pipeline. Draw the forwarding path to avoid the hazard. (5)

```
ADD   R1,R2,R3
SUB   R4,R1,R5
AND   R6,R1,R7
OR    R8,R1,R9
XOR   R10,R1,R11
```

Q4 a) Consider a computer with four stages pipelined. Suppose the stages use a cycle time of 60*ns*, 50*ns*, 90*ns* and 80*ns* respectively. The interface latch for each stage has a delay of 10*ns*. How long will it take to perform 100 instructions? What will be the speedup, efficiency and throughput of the system? (5)

b) What is interconnection network? Draw and explain an eight input general multistage network.

Q5 a) Differentiate between loosely coupled system and tightly coupled system with proper diagram and example. (5)

b) Consider a computer with four floating point processors. Suppose that each processor uses a cycle time of 40ns.How long will it take to perform 400 floating point operations? Is there any difference if the same 400 operations are carried out using one pipeline processor with a cyclic time of 10ns? (5)

Q6 a) What is VLIW architecture? Is it same as super scalar architecture? Justify. (5)

b) Differentiate between arithmetic pipeline and instruction pipeline with example. (5)

Q7

a) What is virtual memory? How a logical address is mapped to physical address in virtual concept? Explain with examples. (5)

b) Differentiate between Super scalar architecture Vs. Super pipelined architecture. (5)

Q8 Write notes on (any two) (5 x 2)

a) Interleave Memory
b) Distributed shared-memory architecture
c) Cluster computers.