Registration no: | | | | | | | | | | |

Total Number of Pages: 02 **M.TECH**

CSPC102

1st Semester Regular / Back Examination – 2016-17

ADVANCED COMPUTER ARCHITECTURE

BRANCH: CSE

Time: 3 Hours

Max marks: 70

Q.CODE:Y844

Answer Question No.1 which is compulsory and any five from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions: (2 x 10)

a) What is the difference between big-endian ordering and little-endian ordering?
b) State Amdahl's law and hence find out the overall speed up in the below givenscenario: "An improvement can speed up 30% of the computation and the improvement makesthe portion affected twice as fast."
c) State at least four differences between a RISC and a CISC based machine.
d) Explain the term speculative execution of instructions.
e) State the advantages of write through policy over write back policy.
f) Explain the terms write allocate and no-write allocate in connection with write miss.
g) State the differences between overlays and virtual memory.
h) What is branch folding?
i) Calculating Overall CPI.

Operation	Frequency	CPI(i)
ALU	40%	1
LOAD	27%	2
STORE	13%	2
BRANCH	20%	5

j) Explain the constraints imposed by control dependences.

Q2 a) Three enhancements with the following speedups are proposed for a new architecture:Speedup1=25, Speedup2 = 35, Speedup3 = 15 Only one enhancement is usable at a time. If enhancement 1 and 2 are each usable for 25% of the time, what fraction of the time must enhancement 3 be used to achieve an overall speedup of 10? (5)

b) Consider the above facts given in question 2(a) and assume, for same benchmark, The possible fraction of use is 15% for each of enhancements 1 and 2 and 70% forenhancement 3. We want to maximize performance. If only one enhancement canbe implemented, which should it be? If two enhancements can be implemented, whichshould be chosen? (5)

Q3 a) We are given a task which is split up into four parts: p1=11%, p2=18%, p3=23%, p4=48%,which add up to 100%. Then we say p1 is not sped up, p2 is sped up 5 times, p3 is sped up20 times and p4 is sped up 1.6 times. Find out the running time and the overall speed up. (5)

b) Assume: (5)

- For 1000 instructions:
  - 40 misses in L1,
  - 20 misses in L2
- L1 hit time: 1 cycle,
- L2 hit time: 10 cycles,
- L2 miss penalty=100
- 1.5 memory references per instruction
- Assume ideal CPI=1.0

Find Local miss rate, AMAT, stall cycles per instruction, and those without L2 cache.

Q4 a) What are the different types of hazard occurred in following instruction? How you can eliminate these hazards. Give proper diagrammatic representation.

```
ADD   R1, R2, R3
SUB   R4, R1, R5
AND   R6, R1, R7
OR    R8, R1, R9
XOR   R10, R1, R11
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b) Suppose:Clock Rate = 200 MHz (5 ns per cycle), Ideal (no misses) CPI = 1.1, 50% arith/logic, 30% load/store, 20% control, 10% of data memory operations get 50 cycles miss penalty1% of instruction memory operations also get 50 cycles miss penalty, Compute AMAT.

Q5 a) Describe VLIW architecture? (5)

b) Differentiate between vector stride and vector length? (5)

Q6 a) Explain delayed branch scheme to avoid instruction hazards. Give suitable example. (5)

b) Explain the different categories of data dependence. What are the possible data hazards that may arise due to these dependence? (5)

Q7 a) With a suitable examples and neat diagrams explain the differences between superscalararchitecture and super pipelined architecture. (5)

b) What do you mean by coherence misses in symmetric shared-memory multiprocessors?Explain the terms true sharing misses and false sharing misses in connection with the above issue.

Q8 Write short notes on any two (5 x 2)

a) Flynn's classification
b) Hyper threading
c) Array processor
d) MIPS