Registration No: | | | | | | | | | | |

Total Number of Pages: 2 **M.TECH**

P1CSBC03

1st Semester Regular Examination 2016-17

Advanced Computer Architecture

BRANCH:CS

Time: 3 Hours

Max Marks: 100

Q.CODE: Y843

Answer Question No.1 which is compulsory and any FOUR from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions: ***Short answer type*** **(2 x 10)**

a) State Amdhal's law. And hence justify the effectiveness of making common case faster.

b) Show the relationship of CPI with the performance of a computer.

c) What is the importance of MFLOP over MIPS in computer designing.

d) What are the addressing modes used in JUMP and ADD R1,R2,R3 ?

e) State the difference between big and little endian representation.

f) Derive the expression of throughput of a pipelined computer.

g) Differentiate between WAW and WAR hazard with examples of each.

h) Enlist the factors affecting "Cache miss" while memory designing.

i) Provide one example of structural hazard caused due to memory accesses.

j) Map NUMA and UMA concepts of computers to Flynn's classification with their justification.

Q2 **a)** Suppose that we are considering an enhancement that runs 10times faster than the original machine but is only usable 40% of the time. What is the overall speed up gained by incorporating the design? **(10)**

b) Describe Flynn's classification with their figure. **(10)**

Q3 **a)** What do you mean by Instruction Set Architecture? Classify the instruction set with respect to operations and addressing fields with example from each. **(10)**

b) Discuss one technique to incorporate instruction level parallelism with an example. **(10)**

Q4 **a)** Describe different Pipeline hazards with their examples. **(10)**

b) Explain two techniques to overcome RAW hazard. **(10)**

Q5 **a)** Write 5 cache optimization techniques and their relevance. **(10)**

b) Suppose that in 1000 memory references there are 40 misses in the first level of cache and 20 misses in the 2nd level of cache. Assuming the miss penalty from the L2 cache to memory is 200 clock cycles, the hit time of L2 cache is 10 clock cycles, the hit time of L1 is 1 clock cycle **(10)**

and there are 1.5 memory references per instruction, calculate average memory access time.

Q6 **a)** Write the use of virtual memory and then justify paged segmentation scheme. **(10)**

b) Describe the techniques to overcome the cache coherence problem. **(10)**

Q7 Write notes on any two. **(10)+(10)**

a) Tomasulo's approach

b) Synchronous Vs Asynchronous Pipelining.

c) RISC architecture.