Registration No: | | | | | | | | | | |

Total Number of Pages: 02

M.TECH
P1ECBC03

1st Semester Regular Examination 2016-17
INTEGRATED CIRCUIT DESIGN
BRANCH: ELECTRONICS AND COMMUNICATION ENGINEERING
Time: 3 Hours
Max Marks: 100
Q.CODE:Y921
Answer Question No.1 which is compulsory and any FOUR from the rest.
The figures in the right hand margin indicate marks.

Q1 Answer the following questions: ***Short answer type*** **(2 x 10)**

a) Define power-delay product and energy-delay product?
b) Draw the small signal equivalent of the stage.
c) 18 cascaded minimum sized transmission gate with an average resistance of 8KΩ capacitances is 3.6fF. Transition from low to high. Find out the propagation delay?
d) State different Test and Diagnostic Equipment?
e) Define Debugability? What is the purpose of focused calibration?
f) State the different mixed signal testing challenges?
g) What is sub threshold current? When does a transistor enter into sub threshold region?
h) Mention the applications of mm-wave ICs?
i) What are current mirrors?
j) Write the scaling technology for small channel devices?

Q2 **a)** i. Design the domino logic for the function F = E+A.(B+C)+G.H **(10)**
ii. Design the 4:1 MUX using Transmission Gate?
b) i. Why nmos switches are used for pulling down a node and pmos switches used for pulling up a node? **(5)**
ii. Explain in detail the issues in dynamic design? **(5)**

Q3 **a)** Inverter in generic 0.25µm technology. $\frac{pMOS}{nMOS}$ = 3.4.Parameters of nMOS transistor are W = 0.375µm, L = 0.25 µm, W/L = 1.25, V_m = 1.25V. Calculate the gain and the noise margins. **(10)**
b) Draw the layout of a four input NAND gate in complementary CMOS. **(5)**
c) What is the output transition probability for N-input static gate? Find out the output transition of 0->1 for a 2-input static CMOS NAND gate and AND gate. **(5)**

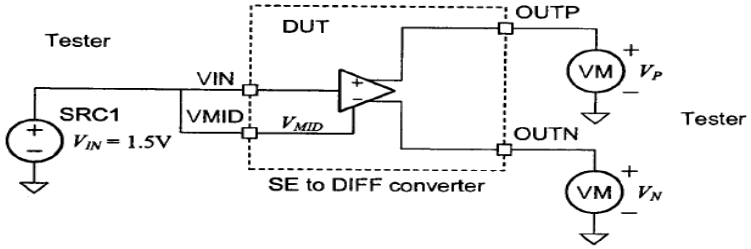
Q4 **a)** Explain with proper circuit diagram the Wilson Current Mirror and Improved Wilson Current Mirror and find out its r_{out} and V_{out}. **(15)**
b) Explain in detail the self biased current reference? **(5)**

Q5 **a)** State the different DC test for digital circuit? **(5)**
b) Define input offset voltage? For a x10 amplifier characterized by $V_{out} = V_{IN}$ = +5V. What is its input and output offset voltage? **(5)**
c) Consider the single-ended to differential converter. The two input of the circuit are labeled OUTP and OUTN. A 1.5V reference voltage V_{MID} is applied to the input of the circuit and ideally, the output should both produce V_{MID}. The **(5)**

voltages at OUTP and OUTN denoted V_P and V_N respectively are measured with a meter producing the following 2 results-

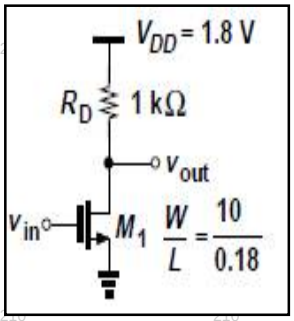
V_P = 1.507V V_N = 1.497V

With the expected output reference level of V_{MID} = 1.5V. Compute the differential and common-mode offsets.



d) Write a short note on floating gate MOS. **(5)**

Q6 **a)** Derive and calculate the small-signal voltage gain of the CS stage shown in Figure below if I_D= 1mA, $\mu_n C_{ox}$=100 μA/V^2, V_{TH}= 0.5 V, and**λ**= 0. Verify that M_1operates in saturation. **(15)**



b) Write a short note on any one **(5)**

(i) FinFET

(ii) POWER MOS

Q7 **a)** Explain the different performance characteristics of OPAMP? **(15)**

b) i. Define load regulation and line regulation? **(5)**

ii. The output of a 5V voltage regulator varies from 5.10V under no-load condition to 4.85V under a 5mA maximum rated load current. What is the load regulation?

iii. The output of a 5V voltage regulator varies from 5.05V-4.95V when the input voltage is changed from 14-6 V under a maximum load condition of 10mA. What is its line regulation?