Registration No: | | | | | | | | | | |

Total Number of Pages: 03 **M.TECH**

P2ARCC07

2nd Semester Regular Examination 2016-17

EMBEDDED SYSTEM DESIGN

Branch : AUTOMATION AND ROBOTICS, COMMUNICATION ENGG, COMMUNICATION SYSTEMS, ELECTRO &INST, COMM. ENGG, ELECTRO AND TELECOMMUNICATION ENGG, SIGNAL PROCESSING AND ENGG, WIRELESS COMMUNICATION TECH.

Time: 3 Hours

Max Marks: 100

Q.CODE:Z809

Answer Question No.1 which is compulsory and any FOUR from the rest.

The figures in the right hand margin indicate marks.

Q1 Answer the following questions: ***Short answer type*** **(2 x 10)**

a) "*Making the system dependable must not be an after-thought, it must be considered from the very beginning*". What do you mean by this statement?

b) With respect to an Automobile give example for a Hard and Soft Real Time embedded system.

c) What do Models of Computations define? Enlist some Models of Computations.

d) Why do we require a Middleware? What are its important characteristics?

e) Given is the logic block for an8 bit register in Figure Q1 e). Write the entity declaration for the following design module.

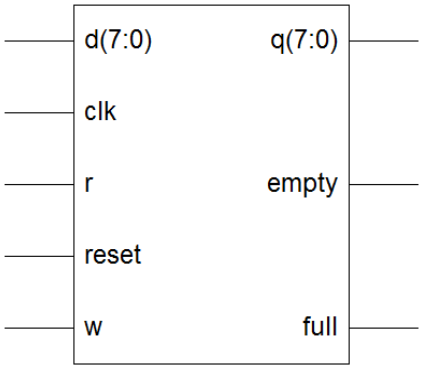

Figure Q1 e)

f) What do you mean by "Co-design''? Mention some Co-Design Tools.

g) Name two Microcontrollers and two RTOS used for Embedded System Design.

h) What are Petrinets? Mention its use.

i) What is use of Ptolemy and Octopus?

j) Under what conditions does the device PIC 16F877 undergoes RESET?

Q2 **a)** Discuss the characteristics and applications of Embedded Systems **(10)**

b) Taking the example of a Biometric Attendance System describe the different hardware components of an Embedded System. **(10)**

Q3 **a)** Design an automatic gel pen vending machine based on FSM model for the following requirement. The machine is initiated by inserting a 10 rupees coin. After inserting the coin, the user can either select "Red", "Green", "Black" or "Blue" pen (to get their choice of pen) or press 'Cancel' to cancel the order and take back the coin. **(10)**

b)(i) Given in Figure Q3 b (i) is an example of a Process that has been represented using SDL. Draw its FSM (State Chart) equivalent. **(5)**

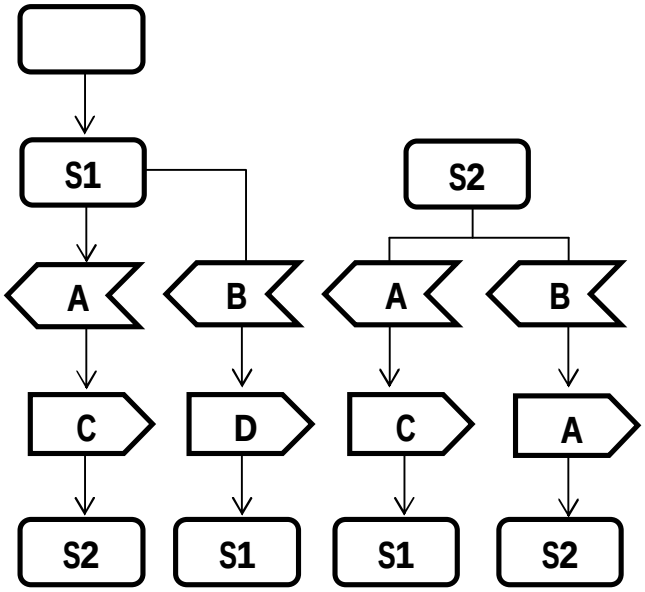

Figure Q3 b (i)

b(ii) For the given FSM in Figure Q3 b (ii), classify the different states like Super states, Basic State, Ancestor state, AND Super states and OR Super states. **(5)**

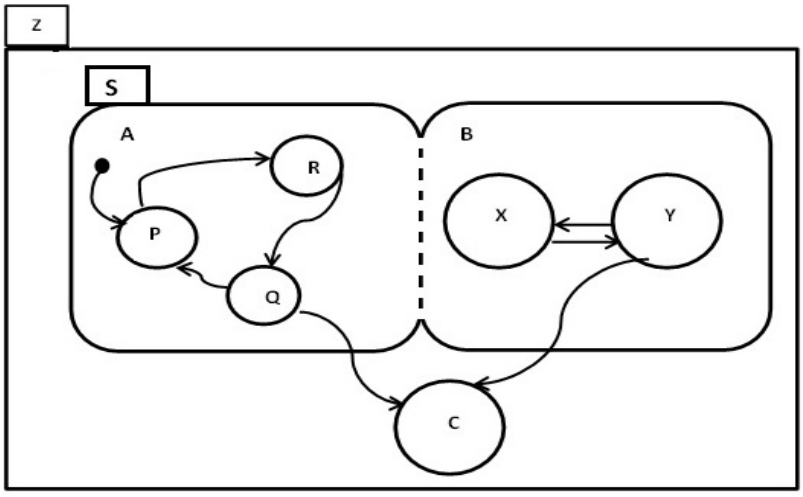

Figure Q3 b (ii)

If you were to design a simple Mobile Phone and represent it as the above FSM then what names can you give to different states A,B,C,P,Q,R,X,Y,S and Z.

Q4 **a)** A system consists of three periodic tasks: (3, 1), (5, 2), and (8, 3). What is the total utilization? Construct an EDF and RM schedule for this system in the interval (0, 32). Label any missed deadlines. **(10)**

b) Three processes with ID P1, P2, P3 with execution times of 7, 6, 11 ms respectively enters the ready queue together in the order P3, P1, P2. Calculate the above parameters using RR scheduling. (No I/O waiting time present for any process).Time Slice=3ms. Calculate the Waiting time and Turn Around Time (TAT) for each process and the average waiting time and Average Turn Around Time (TAT) for these processers. **(10)**

Q5 **a)** Draw a logic diagram using simple gates and a 4:1 multiplexor that is equivalent to the VHDL code shown below. Be sure to label all the inputs of your multiplexor correctly. **(10)**

```
library IEEE;
use IEEE.std_logic_1164.all;
entity heat_ckt is
port (temp, sun, humid: in std_logic;
day: in std_logic_vector (1 downto 0);
dry, dehydrate: out std_logic);
end heat_ckt;
architecture arch of heat_ckt is
begin
dehydrate <= (humid or temp) and (not sun);
dry <= (sun xor humid) when day = “00” else
humid when day = “01” else
sun and temp;
end arch;
```

b) Given is the logic representation of a 4 bit adder/ subtractor in Figure Q5b). Write a VHDL code to implement the same. **(10)**

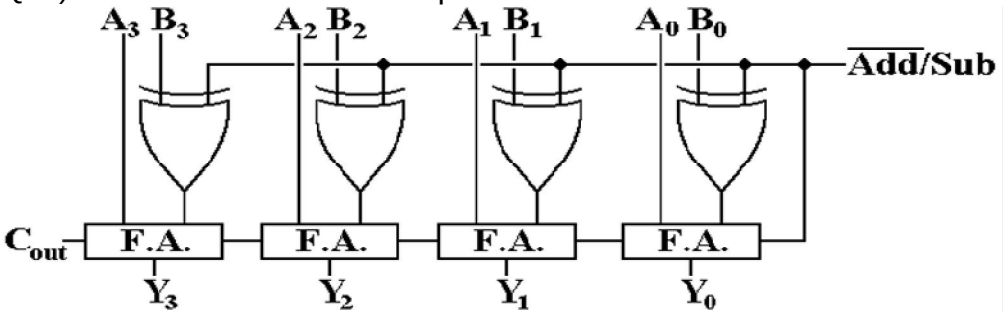

Figure Q5 b)

Q6 **a)** A data-flow graph (DFG) is a graph which represents data dependency between a number of operations. Any algorithm consists of a number of ordered operations. Draw the DFG for finding the root of a quadratic equation ; Given- **(10)**

$t_1 = a*c;$
$t_2 = 4*t1;$
$t_3 = b*b;$
$t_4 = t_3 - t_2;$
$t_5 = sqrt(t_4);$
$t_6 = -b;$
$t_7 = t_6 - t_5;$
$t_8 = t_7 + t_5;$
$t_9 = 2*a;$
$r_1 = t_7/t_9;$
$r_2 = t_8/t_9;$

b) Discuss the Priority Inversion and Priority Inheritance protocols with suitable illustrations. **(10)**

Q7 **Elaborate on any two of the following** **(10X2)**

a) Different Modeling Styles of VHDL
b) UML Diagrams
c) ARM Processor
d) Different Phases of EDLC