

Registration no:

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Total Number of Pages: 01

**M.TECH**  
**EEPE206**

**2<sup>nd</sup> Semester Back Examination – 2016-17**

**EMBEDDED SYSTEM**

**BRANCH(S): ELECTRIC & ELECTRONIC ENGG (POWER SYSTEM ENGG), ELECTRICAL POWER SYSTEM, INFORMATION TECH., POWER SYSTEM ENGG, POWER SYSTEMS**

**Time: 3 Hours**

**Max Marks: 70**

**Q.CODE:Z1194**

**Answer Question No.1 which is compulsory and any five from the rest.  
The figures in the right hand margin indicate marks.**

- Q1 Answer the following questions: (2 x 10)**
- a) What is a real time operating system. Give one example.
  - b) What are the constraints of the codesign tool.
  - c) What does it take to make an OS an RTOS ?
  - d) What is maximum lateness.
  - e) What do you mean by task graphs. Give one example of task graph.
  - f) Define electrical robustness.
  - g) What is dynamic voltage scaling.
  - h) Why timer circuits are required in embedded system design.
  - i) Dynamic power management states of the StrongArm Processor SA 1100.
  - j) What is the difference between the PIC and AVR microcontrollers.
- Q2 a) What is the function of A/D converters in embedded system. Explain the sample-and-hold circuit. (5)**
- b) Explain the IMEC design flow. (5)**
- Q3 Describe synchronization and communication for designing an embedded system ? What is message passing ? Explain the various message passing techniques with example. (10)**
- Q4 Explain the embedded development life cycle (EDLC) with proper block diagram. (10)**
- Q5 a) What do you mean by state charts ? Describe the state oriented behavior of the state charts with finite state machines. (5)**
- b) Explain the modelling delay in VHDL. (5)**
- Q6 a) What is scheduling algorithms? Explain the aperiodic scheduling algorithms? (5)**
- b) What is VHDL modelling. Explain the modelling of sequential logic. (5)**
- Q7 a) What is SDL ? Explain the graphical representation with finite state machines. (10)**
- Q8 Write short notes on (any two) (5 x 2)**
- a) Codesign Tool (COOL)
  - b) The OCTOPUS design flow
  - c) UML
  - d) Advanced features of VHDL