QP Code: R262B006 | Reg. No | | | | | | | | | | | AY 25

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

M.Tech. (Second Semester) Regular Examinations, May – 2026

24MVLPC12001 - System on Programmable Chip Design

(ECE-VLSI)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	What does IP mean in VLSI?	CO2	K2
b.	Differentiate between emulation and FPGA prototyping.	CO1	K2
c.	Describe a real-time processing operating system.	CO3	K2
d.	Identify the three major components of FPGA architecture.	CO4	K3
e.	List the four layers of application architecture.	CO3	K1

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2.a	Describe the instruction set architecture (ISA) with relevant classification and examples.	5	CO1	K3
b	Differentiate between Von Neumann and Harvard architectures.	5	CO1	K2
	(OR)			
c	Explain the significance of pipeline stages and the concept of instruction throughput.	5	CO1	K3
d	Illustrate the use of register transfer language (RTL) in processor design.	5	CO1	K3
3.a.	Describe clock domain crossing issues and synchronization methods in digital systems.	5	CO2	K4
b	Discuss types of hazards in pipeline architecture and their resolution techniques.	5	CO2	K3
	(OR)			
c.	Briefly explain different types of IP cores and their relevance in modern VLSI design.	5	CO3	K5
d.	Explain the role of FPGA-based SoC systems in prototyping embedded applications.	5	CO3	K3
4.a.	Illustrate the process of system-level design flow using IP integration methodology.	10	CO3	K4
	(OR)			
b.	Analyze AMBA and its role in SoC interconnect architecture.	10	CO3	K4
5.a	Differentiate between a peripheral and an interface with suitable examples.	5	CO4	K3
b	Elaborate on the purpose and structure of a core wrapper in DFT methodology.	5	CO4	K4
	(OR)			
c	Describe the function of embedded RTOS in managing real-time SoC applications.	5	CO4	K3
d	Discuss the concept of isolation techniques for IP security in SoC design.	5	CO4	K4

6.a	Provide a comprehensive overview of the IEEE P1500 standard for embedded core testing.	5	CO1	K5
b	Discuss pipelining and its effects on instruction-level parallelism.	5	CO1	K3
	(OR)			
c.	Describe the functionality and advantages of scan-based DFT techniques.	5	CO1	K4
d	Explain the role of boundary scan (JTAG) in test access mechanisms.	5	CO1	K3

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