QP Code: R261B018 | Reg. No | | | | | | | | | | | AY 25

Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)

M.Tech. (Second Semester - Regular) Examinations, May – 2026

24MVLPC12002 – VLSI Signal Processing

Time: 3hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a. List the characteristics of systolic architecture.	CO1	K2
b. Differentiate between bit-level architecture and redundant arithmetic.	CO2	K2
c. Define Bit-serial arithmetic.	CO3	K3
d. Explain retiming and unfolding in VLSI signal processing.	CO4	K1
e. Define digital signal processors (DSPs).	CO5	K1

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions	Marks	CO #	Blooms Level
2. a. Explain the importance of designing low-power lattice filters in modern VLSI systems.	5	CO1	K3
b. Describe the characteristics and design challenges of FIR filter structures.	5	CO1	K4
(OR)			
c. Write short notes on: (i) Iteration Bound (ii) Algorithmic Strength Reduction.	5	CO1	K2
d. Discuss the challenges in implementing parallelism in programmable DSP architectures.	5	CO1	K3
3.a. Explain critical path in VLSI DSP systems and discuss its effect on the maximum clock frequency.	5	CO2	K3
b. Explain the differences between synchronous and asynchronous pipelines.	5	CO2	K4
(OR)			
c. Discuss the role of parallelism in achieving performance in real-time signal processing applications.	5	CO2	K3
d. Differentiate between retiming and unfolding with respect to throughput optimization.	5	CO2	K4
4.a. Evaluate the use of loop unrolling and loop pipelining for real-time DSP system design.	5	CO3	K3
b. Describe the use of recursive filters in feedback-based DSP system implementation.	5	CO3	K2
(OR)			
c. Describe distributed arithmetic and explain its application in efficient FIR filter implementation.	5	CO3	K2
d. Explain folding transformation in VLSI DSP architectures and discuss how it reduces hardware complexity.	5	CO3	K3
5.a. Explain systolic array architecture and discuss its advantages in high-speed VLSI signal processing	5	CO4	K2

b.	Describe how clock domain crossing is handled in pipelined VLSI signal processing systems.	5	CO4	K3
	(OR)			
c.	Contrast adaptive filters and recursive filters with examples from VLSI implementations.	5	CO4	K2
d.	Explain the concept and design impact of redundant architecture in low-latency systems.	5	CO4	K2
6.a.	Discuss the design challenges of implementing fault-tolerant VLSI DSP systems.	5	CO5	K4
b.	Explain how bit-serial and bit-parallel architectures differ in terms of area and speed.	5	CO5	K3
	(OR)			
c.	Explain the concept of asynchronous pipelining and its significance in power-sensitive VLSI systems.	5	CO5	K2
d.	Describe how systolic arrays are used in VLSI DSP and mention their advantages	5	CO5	K3

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