QP Code: R264A031 | Reg. No | | | | | | | | | | | AY 23

Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)

B. Tech (Fourth Semester – Regular/Supplementary) Examinations, April 2026

23BELPC24004/ 23BEEPC24004 – Analog and Digital Circuits

(EE/EEE)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	Explain the procedure to perform subtraction using 2's complement method with an example.	CO3	K2
b.	What do you mean by sequential logic circuit?	CO3	K2
c.	State the difference between counter and shift register in digital logic circuit.	CO5	K1
d.	Draw the series voltage regulator with circuit diagram.	CO1	K2
e.	State the truth table of J-K flip-flop.	CO4	K1

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2. a.	Derive the expression for output of non-inverting amplifier.	5	CO2	K2
b.	Design a subtractor circuit that $V_0=3V_1+2V_2-4V_3$	5	CO2	K3
	(OR)			
c.	Describe and illustrate a differential amplifier with its circuit diagram.	5	CO2	K2
d.	Explain the concept of Common Mode Rejection Ratio (CMRR) of an OPAMP. Compare ideal and practical op-amp characteristics.	5	CO2	K2
3.a.	Explain the construction and working of a half subtractor. Derive expressions for Difference and Borrow output.	5	CO3	K3
b.	Design the Binary to Grey and Grey to Binary code converter logic diagram with an example.	5	CO3	K2
	(OR)			
c.	Explain the demultiplexer (DEMUX) with diagram and describe the operation of a 1:4 demultiplexer.	5	CO3	K3
d.	Explain the half adder circuit with logic diagram, truth table, and Boolean expression.	5	CO3	K3
4.a.	Draw the truth table and characteristic equation of a J-K flip flop. Explain how it removes the forbidden state of the S-R flip flop.	5	CO4	K2
b.	Explain how a T flip-flop can be realized from a J-K flip-flop. Derive its truth table and characteristic equation.	5	CO4	K3
	(OR)			
c.	Describe and working of a master–slave J-K flip flop. Show how the two stages (master and slave) are controlled by complementary clock signals and how this avoids race around.	5	CO4	K2
d.	Explain in detail how to convert a J-K flip-flop into a D-flip-flop. Derive the required input equations and draw the logic diagram.	5	CO4	K3

5.a.	Design a mod-9 asynchronous counter using flip-flops.	5	CO5	K4
b.	Draw and explain a 4-bit SISO shift register.	5	CO5	K2
	(OR)			
c.	Design a decade asynchronous counter and explain its operation.	5	CO5	K4
d.	Explain 3-bit synchronous counter with diagram and operation	5	CO5	K2
6.a.	Explain NAND and NOR gates as universal gates. Realize AND, OR, and NOT gates using NAND gate only.	5	CO3	K3
b.	Explain 1's complement and 2's complement subtraction methods. Perform the subtraction $(25)_{10} - (37)_{10}$ using 2's complement method.	5	CO3	K3
	(OR)			
c.	State and prove De Morgan's theorems using Boolean algebra. Implement them using logic gate diagrams	5	CO3	K4
d.	Simplify the Boolean function using 4-variable K-map: $F(A, B, C, D) = \Sigma m (0,2,5,7,8,10,13,15)$	5	CO3	K3

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