Gandhi Institute of Engineering and Technology University, Odisha, Gunupur (GIET University)

M. Tech. (Third Semester - Regular) Examinations, December – 2025

24MVLPE23001 - MOS Devices Modelling and Characterization

Time: 2 hrs Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	What is the depletion approximation in MOS electrostatics?	CO1	K2
b.	Define interface trap charges at the Si–SiO2 interface.	CO2	K2
c.	Define weak inversion (subthreshold conduction) in a MOSFET.	CO3	K2
d.	What is meant by a small-signal model of a transistor?	CO4	K2
e.	What is Drain Induced Barrier Lowering (DIBL)?	CO5	K2

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2. a.	Starting from Poisson's equation, derive expressions for surface potential and depletion width in a MOS capacitor under depletion approximation.	5	CO1	K3
b.	Explain how the work function difference between metal and semiconductor affects the flat-band condition in a MOS structure.	5	CO1	K3
	(OR)			
c.	Discuss the effect of oxide thickness and substrate doping on the electrostatic behaviour of a MOS capacitor.	5	CO1	K4
d.	Explain the significance of midgap condition in MOS electrostatics and its relevance to threshold voltage.	5	CO1	K4
3.a.	Describe how C–V measurements can be used to extract oxide capacitance and interface trap density.	5	CO2	K3
b.	Explain the dependence of threshold voltage on oxide thickness, substrate doping concentration and fixed oxide charge.	5	CO2	K3
	(OR)			
c.	Discuss the effect of body bias on the surface potential and threshold voltage with appropriate equations.	5	CO2	K4
d.	Explain how non-ideal C–V curves can be interpreted to diagnose process-induced defects in MOS devices.	5	CO2	K4
4.a.	Discuss the influence of temperature on MOSFET parameters such as threshold voltage, mobility and leakage current.	5	CO3	K3
b.	Explain different breakdown mechanisms in MOS devices, including oxide breakdown and junction breakdown.	5	CO3	K3
	(OR)			

c.	Compare current–voltage models for strong inversion and weak inversion, highlighting their regions of validity and applications.	5	CO3	K4
d.	Explain how moderate inversion is modelled and why it is important for low-power and analog circuit design.	5	CO3	K4
5.a.	Explain the switching characteristics of a MOSFET used in digital logic, describing rise time, fall time and propagation delays.	5	CO4	K3
b.	Describe how the charge control concept is used in modelling transient switching of MOSFET-based inverters.	5	CO4	K3
	(OR)			
c.	Compare small-signal and large-signal models in terms of their applications in analog and digital circuit design.	5	CO4	K4
d.	Explain how device capacitances influence the speed and power dissipation of MOS logic circuits.	5	CO4	K4
6.a.	Discuss quantum mechanical effects in ultra-thin oxide MOS devices, including tunnelling and quantization of energy levels.	5	CO5	K3
b.	Explain different leakage mechanisms in scaled MOSFETs such as DC gate current, junction leakage and band-to-band tunnelling.	5	CO5	K3
	(OR)			
c.	Describe Gate-Induced Drain Leakage (GIDL) and explain how device design can minimize its impact.	5	CO5	K4
d.	Discuss MOSFET scaling principles and highlight the major challenges in continuing classical scaling into deep-submicron and nanometer regimes.	5	CO5	K4

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