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AY 24

Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)

M.Tech. (First Semester – Regular/ Supplementary) Examinations, January – 2026

24MVLPC11002 – Digital IC Design
(ECE-VLSI)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions
(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ALL questions	CO #	Blooms Level
a. Define MOSFET threshold voltage (Vth).	CO1	K1
b. Define static CMOS logic and mention one key advantage.	CO2	K1
c. Define latch and register (flip-flop).	CO3	K1
d. Define datapath circuit.	CO4	K1
e. Define ROM and mention one application.	CO5	K1

PART – B **(10 x 5 = 50 Marks)**

Answer ALL the questions	Marks	CO #	Blooms Level
2. a. Explain MOSFET I–V characteristics under static conditions and describe Id expressions in triode and saturation.	5	CO1	K4
b. Discuss MOSFET secondary effects (body effect, CLM, DIBL, velocity saturation) and their impact on digital circuits.	5	CO1	K4
(OR)			
c. Explain CMOS inverter static characteristics. Define VIL, VIH, VOH, VOL and noise margins.	5	CO1	K4
d. Explain CMOS inverter dynamic behavior using RC delay model. Describe rise/fall times and propagation delay.	5	CO1	K4
3.a. Explain static CMOS design methodology for complex gates. Construct PUN/PDN for a given Boolean function.	5	CO2	K4
b. Compare logic styles (static CMOS, pseudo-NMOS, pass-transistor, transmission gate) with pros/cons.	5	CO2	K5
(OR)			
c. Explain logical effort for complex gates. Illustrate g and p for NAND/NOR and interpret delay.	5	CO2	K4
d. Discuss delay and power trade-offs of complex gates including input capacitance and stacking effects.	5	CO2	K5
4.a. Explain transmission-gate based latch and edge-triggered register operation with timing waveforms.	5	CO3	K4
b. Explain dynamic latches/registers and discuss leakage, charge sharing, and clock feedthrough effects.	5	CO3	K4
(OR)			
c. Derive setup and hold constraints for a register-to-register path including skew and uncertainty.	5	CO3	K4
d. Discuss timing issues: metastability, skew, jitter, and their impact on high-speed design.	5	CO3	K5

5.a.	Compare ripple-carry and carry-lookahead adders in terms of delay, area, and wiring.	5	CO4	K5
b.	Explain carry-select and carry-skip adders. Discuss design choices for different word lengths.	5	CO4	K4
	(OR)			
c.	Design an accumulator using adder and register. Explain timing and overflow considerations.	5	CO4	K6
d.	Explain array multiplier architecture and partial product accumulation.	5	CO4	K4
6.a.	Explain ROM architecture and ROM cell operation. Compare common ROM styles conceptually.	5	CO5	K4
b.	Explain read-write memory organization: decoder, cell array, precharge, sense amps, and write drivers.	5	CO5	K3
	(OR)			
c.	Describe DRAM cell and dynamic memory design. Explain refresh requirement and timing parameters.	5	CO5	K4
d.	Explain 6T SRAM cell. Discuss read stability and write ability and the role of transistor sizing.	5	CO5	K5

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