

**Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)**



M.Tech. (First Semester – Regular/Supplementary) Examinations, January – 2026
24MVLPE11011 – Analog IC Design

Time: 3 hrs

Maximum: 60 Marks

**Answer ALL questions
(The figures in the right hand margin indicate marks)**

PART – A

(2 x 5 = 10 Marks)

Q.1. Answer ALL questions	CO #	Blooms Level
a. Define threshold voltage (V_{th}) and mention one factor that affects it.	CO1	K2
b. List two limitations of a basic MOS current mirror.	CO3	K1
c. What is Miller capacitance and how is it ‘seen’ at the input?	CO4	K2
d. Define slew rate.	CO5	K2
e. List the four basic feedback topologies.	CO5	K1

PART – B

(10 x 5 = 50 Marks)

Answer ALL the questions

	Marks	CO #	Blooms Level
2. a. Explain source follower operation and obtain voltage gain, input/output resistance. Mention its typical applications.	5	CO2	K3
b. Explain common-gate amplifier and derive gain and input resistance. Compare with CS for wideband use.	5	CO2	K4
(OR)			
c. Describe cascode amplifier operation, derive output resistance enhancement, and explain gain improvement.	5	CO2	K4
d. Design a single-stage MOS amplifier for a specified gain and output swing (outline steps and key constraints).	5	CO2	K6
3.a. Explain supply-insensitive biasing circuits and show how PSRR is improved in bias generation (conceptual).	5	CO3	K4
b. Describe temperature-insensitive biasing approaches (PTAT/CTAT reference combination) and explain operating principle.	5	CO3	K4
(OR)			
c. Analyze the impact of mismatch on current mirrors and differential pairs; explain Pelgrom’s model qualitatively.	5	CO3	K4
d. Design a bias network meeting a target current over PVT variations; outline design steps and validation checks.	5	CO3	K6
4.a. Discuss design of a multistage amplifier: gain distribution, pole placement, and stability concerns.	5	CO4	K5
b. Compare CS, CG, and cascode stages for wideband design; justify which stage is preferred and why.	5	CO4	K5
(OR)			
c. Explain the need for buffering in multistage amplifiers and how source followers help in driving capacitive loads.	5	CO4	K4
d. Propose a two-/three-stage amplifier architecture for a target DC gain and bandwidth; provide a clear design flow.	5	CO4	K6
5.a. Explain slew rate, its dependence on bias current and compensation capacitor, and how to improve it.	5	CO5	K4
b. Discuss PSRR and CMRR: definitions, measurement idea, and circuit design strategies to improve them.	5	CO5	K5

(OR)

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| c. | Explain noise in op-amps (thermal and 1/f) and discuss how sizing and biasing affect input-referred noise. | 5 | CO5 | K4 |
| d. | Describe design considerations for high-speed op-amps: gain-bandwidth, compensation, output stage, and load driving. | 5 | CO5 | K5 |
| 6.a. | Discuss advanced compensation techniques (nulling resistor, feedforward, pole-splitting) and when they are used. | 5 | CO5 | K5 |
| b. | Analyze the trade-off between stability and speed (UGB vs phase margin) and how design choices influence both. | 5 | CO5 | K5 |

(OR)

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| c. | Explain how slew rate and large-signal behavior interact with compensation capacitor and bias current. | 5 | CO5 | K4 |
| d. | Design a compensated two-stage op-amp for a target UGB and phase margin; provide a structured design procedure. | 5 | CO5 | K6 |

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