Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)

B. Tech (Fifth Semester - Regular) Examinations, November 2025

23BECPC35003-Digital VLSI Design

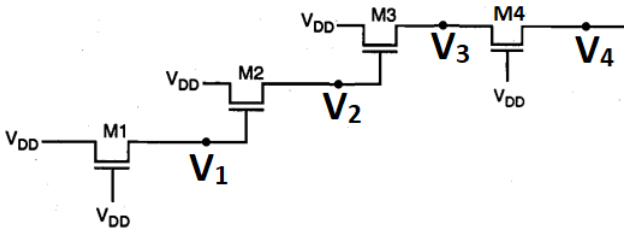
(Electronics and Communication Engineering)

Time: 3 hrs Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a. Define netlist in VLSI design.	CO1	K1
b. What is the Gradual Channel Approximation in a MOSFET, and why is it used in the analysis of device operation?	CO2	K2
c. Explain in short the condition of operating n-MOSFET in linear and saturation region.	CO3	K2
d. Analyze the given circuit and find the voltage V_1, V_2, V_3, and V_4. Consider the threshold voltage for nMOS transistor M1, M2, M3, and M4 as V_{TH1}, V_{TH2}, V_{TH3}, and V_{TH4} respectively. 	CO4	K4
e. Explain in brief Precharge-Evaluate Logic.	CO5	K2

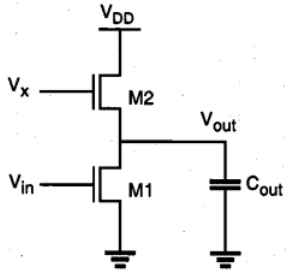
PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions	Marks	CO #	Blooms Level
2. a. Explain the fabrication steps for n-type metal oxide semiconductor field effect transistor.	5	CO1	K2
b. Explain with neat diagram photolithography process in semiconductor fabrication?	5	CO1	K2
(OR)			
c. Explain VLSI design styles with neat diagram.	5	CO1	K2
d. Draw the stick diagram of CMOS inverter.	5	CO1	K3
3.a. Explain the accumulation and inversion in pMOSFET with applied voltage.	5	CO2	K2
b. What are the advantages of CMOS logic circuit? Discuss the advantages with respect to other logic circuit.	5	CO3	K2
(OR)			
c. Explain steps of top down approach for VLSI logic circuit design.	5	CO3	K3
d. What is second order effect in nMOSFET. Write the expression for V_{TH}, and I_D considering the second order effect.	5	CO2	K3
4.a. Implement the Boolean expression **(AB+C(D+E))** by using nMOS depletion type load.	5	CO4	K3
b. Explain the working principle of CMOS transmission gate.	5	CO3	K2

(OR)

c.	What is parasitic capacitance in CMOS circuit? Explain with considering CMOS inverter circuit.	5	CO4	K2
d.	Explain the working of CMOS NAND gate for 2 input with neat circuit diagram.	5	CO3	K2
5.a.	Draw the clocked CMOS SR-latch circuit based on NOR gate and explain its function and write the corresponding truth table.	10	CO4	K3

(OR)

b.	Consider a resistive load n-MOS inverter circuit with $\mathbf{V_{DD} = 5\ V, K'n = 20\ \mu A/V^2, V_{T0} = 0.7\ V, R_L = 200\ k\Omega, \&\ W/L = 1}$. Calculate the critical voltage ($\mathbf{V_{OL}}$, $\mathbf{V_{OH}}$, $\mathbf{V_{IL}}$,$\mathbf{V_{IH}}$) and find the noise margin of the circuit.	10	CO4	K3
6.a.	Explain voltage bootstrapping method for the given circuit and find the Cboot/Cs ratio. 	6	CO5	K3
b.	Draw the circuit diagram and explain the working of three-stage Enhancement-load dynamic shift register (ratioed logic).	4	CO6	K2

(OR)

c.	Design the circuit for expression **A.(D + E) + B.C** , where (*A, B, C, D,* and *E* are the inputs for the circuit) considering: i) CMOS Logic ii) Domino CMOS logic	6	CO5	K3
d.	Draw the circuit diagram for the expression $\boldsymbol{F = AS + B\overline{S}}$ using Pass gate.	4	CO6	K2

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