QP Code: R252B060 | Reg. No | | | | | | | | | | | AY 24

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

M.Tech. (Second Semester) Regular Examinations, July – 2025

24MVLPC12002 - VLSI Signal Processing

(ECE-VLSI)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	Define iteration bound.	CO2	K2
b.	Explain retiming and unfolding in VLSI signal processing.	CO1	K2
c.	Enumerate four uses of parallel processing.	CO3	K2
d.	Explain the advantage of lattice filter structure.	CO3	K2
e.	Define digital signal processors (DSPs).	CO4	K3

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2.a	Discuss the challenges associated with implementing parallelism in VLSI signal processing systems.	5	CO1	K3
2.b	Explain pipelining and parallel processing in VLSI and compare them with suitable examples.	5	CO1	K2
	(OR)			
2.c	Write a short note on instruction-level parallelism and its limitations in VLSI signal processing.	5	CO1	K3
2.d	Differentiate between static and dynamic pipelining with examples from signal processor designs.	5	CO1	K2
3.a	Explore the role of parallel processing in real-time VLSI systems with an example use case.	5	CO2	K3
3.b	Differentiate between retiming and unfolding in VLSI signal processing and explain their effects on speed.	5	CO2	K4
	(OR)			
3.c	Discuss loop unrolling as a throughput enhancement technique in VLSI design.	5	CO2	K4
3.d	Describe how clock domain crossing is handled in pipelined VLSI signal processing systems.	5	CO2	K3
4.a	List and explain five real-world applications of VLSI signal processing.	5	CO3	K5
4.b	Discuss the advantages and limitations of pipelining and parallelism in high-performance DSP systems.	5	CO3	K3
	(OR)			
4.c	Explain the concept of hardware-software co-design in VLSI signal processing applications.	5	CO3	K4
4.d	Describe the design trade-offs in fixed-point vs floating-point architecture for VLSI DSP.	5	CO3	K4
5.a	Contrast adaptive filters and recursive filters with examples from VLSI implementations.	5	CO4	K3

5.b	Explain the concept and design impact of redundant architecture in low-latency systems.	5	CO4	K4
	(OR)			
5.c	Discuss the design challenges of implementing fault-tolerant VLSI DSP systems.	5	CO4	K3
5.d	Explain how bit-serial and bit-parallel architectures differ in terms of area and speed.	5	CO4	K4
6.a	Elaborate on the lattice filter structure with a focus on modular VLSI design.	5	CO2	K5
6.b	Explain the concepts of data parallelism and task parallelism in parallel DSP VLSI architectures.	5	CO2	K3
	(OR)			
6.c	Explain the concept of asynchronous pipelining and its significance in power-sensitive VLSI systems.	5	CO2	K4
6.d	Describe how systolic arrays are used in VLSI DSP and mention their advantages.	5	CO1	K2

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