QP Code: R252B050 | Reg. No | | | | | | | | | | | AY 24

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

M.Tech. (Second Semester) Regular Examinations, July – 2025

MPCEC2010 - System on Programmable Chip Design

(ECE-VLSI)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	Explain the basic bus architecture in SoC.	CO1	K2
b.	Define IP in VLSI.	CO1	K1
c.	List the 4 layers of application architecture.	CO2	K2
e.	Discuss peripheral interface and its relevance to SoC testing.	CO3	K2
f.	Differentiate between PCIe and AMBA.	CO4	K2

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2.a	Explain the working and purpose of IEEE P1500 standard in SoC testability.	5	CO1	K3
b	Describe the concept of pipelining and its impact on instruction execution.	5	CO1	K2
	(OR)			
c	Illustrate the use of scan chains and boundary scan for chip-level testing.	5	CO1	K3
d	Discuss Built-In Self-Test (BIST) techniques and their advantages in VLSI testing.	5	CO1	K4
3.a	Differentiate between NoC and SoC with relevant architectural features.	5	CO2	K3
b	Explain routing algorithms used in packet-switched NoC systems.	5	CO2	K4
	(OR)			
c	Describe the role of memory hierarchy and cache coherence in multiprocessor SoC.	5	CO2	K4
d	Analyze clock domain crossing issues and mitigation strategies in synchronous SoC design.	5	CO2	K4
4.a	Describe instruction set architecture (ISA) and its influence on processor design.	5	CO3	K5
b	Explain the role of AMBA protocols in SoC design and integration.	5	CO3	K3
	(OR)			
c	Evaluate the importance of hardware/software co-design in embedded systems.	5	CO3	4.c
d	Discuss the types and use cases of on-chip interconnect topologies.	5	CO3	4.d
5.a	Explain the IP life cycle management process in SoC-based development.	5	CO4	5.a
b	Discuss various low-power design techniques used in advanced SoC development.	5	CO4	5.b
	(OR)			
c	Analyze the impact of thermal management and heat dissipation in SoC packaging.	5	CO4	K4
d	Describe the architecture and functions of a real-time operating system (RTOS) in embedded SoCs.	5	CO4	K3

6.a	Describe the purpose and functioning of cache memory in enhancing SoC processor performance.	5	CO2	K5
b	Explain the role of memory interleaving in reducing latency and improving bandwidth.	5	CO2	K3
	(OR)			
c	Discuss various types of SoC memory technologies and their comparative benefits.	5	CO2	K4
d	Analyze the impact of pipeline hazards and solutions to overcome them.	5	CO2	K4

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