QP Code: R252B080 | Reg. No | | | | | | | | | | | AY 24

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

M.Tech. (Second Semester) Regular Examinations, July – 2025

24MECPE12002/24MVLPE1200 - IC Technology

(ECE/ ECE-VLSI)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

	Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a	What are the various methods used for wafer preparation, and what are the specifications typically associated with semiconductor wafers?	CO1	K2
b	Describe the various techniques of epitaxy used in semiconductor manufacturing.	CO2	K3
c	Discuss the concept of diffusion in semiconductor materials and its relevance in device fabrication.	CO2	K2
d	Define semiconductor measurements: conductivity type, resistivity, and Hall effect measurements.	CO4	K1
e	What are the components of packaging in semiconductor devices, and what is electronics package reliability?	CO4	K2

PART – B **(10 x 5 = 50 Marks)**

	Answer ***ALL*** the questions	Marks	CO #	Blooms Level
2.a	Discuss the significance of semiconductor substrate phase diagrams and solid solubility in manufacturing processes, and how they influence material selection and device performance.	5	CO1	K2
2.b	Examine crystal growth techniques like Czochralski and Bridgman growth of GaAs, highlighting their contributions to high-quality substrate production.	5	CO1	K3
	(OR)			
2.c	Explain the process of silicon wafer cleaning and its role in ensuring contamination-free fabrication.	5	CO1	K2
2.d	Describe different etching techniques in VLSI processing and compare their precision and impact on reliability.	5	CO1	K3
3.a	Explain the deposition methods: evaporation, sputtering, and chemical vapor deposition, their advantages and applications.	5	CO2	K4
3.b	Compare epitaxial layers formed through MBE, VPE, and LPE techniques.	5	CO2	K5
	(OR)			
3.c	Describe rapid thermal processing (RTP) and its benefits in controlling thermal budgets.	5	CO2	K4
3.d	Explain oxidation in device fabrication and differentiate between dry and wet oxidation.	5	CO2	K2
4.a	Explain device isolation methods: junction, oxide, and trench isolation.	5	CO3	K3
4.b	Explore Schottky, Ohmic contacts, and metallization in semiconductor packaging.	5	CO3	K3
	(OR)			
4.c	Discuss VLSI packaging techniques: flip-chip, wire bonding, and TAB.	5	CO3	K4
4.d	Explain CMOS latch-up and strategies to prevent it.	5	CO3	K3

5.a	Define packaging in semiconductor devices and factors affecting reliability.	5	CO4	K4
5.b	Discuss the importance of packaging for quality and reliability in semiconductor devices.	5	CO4	K5
	(OR)			
5.c	Describe the relevance of Hall effect measurements in semiconductor characterization.	5	CO4	K3
5.d	Explain thermal and electrical design considerations in semiconductor packaging.	5	CO4	K4
6.a	Describe the CMOS process flow including N-well, P-well, and Twin tub technologies.	5	CO3	K3
6.b	Discuss GaAs technologies: MESFET, MMIC, MODFET, and optoelectronic devices.	5	CO3	K3
	(OR)			
6.c	Outline silicon bipolar technologies: second-order effects, BJT performance, and BiCMOS.	5	CO1	K3
6.d	Explain conductivity type and resistivity measurements in substrate quality assessment.	5	CO4	K2

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