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GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

Ph.D. (First Semester-Winter) Examinations, June – 2025

23WPPEEC1012 – Analog and Digital CMOS VLSI Design

(ECE)

Time: 3 hrs Maximum: 70 Marks

The figures in the right hand margin indicate marks.

	Answer *ANY FIVE* Questions. (14 x 5 = 70 Marks)	**Marks**
1.a.	Discuss the concept of robustness in digital circuits. How can designers ensure that circuits are robust against variations?	8
b.	Describe the physical design flow, including the steps of floor planning, placement, and routing.	6
2.a.	Describe the human body model and machine model for ESD protection.	8
b.	Discuss the concept of cascading dynamic gates and the role of CMOS transmission gate logic.	6
3.a.	What is the bi-stability principle in static latches? How does it relate to the operation of master-slave edge-triggered registers?	7
b.	What are the key differences between static SR flip-flops and master-slave edge-triggered registers?	7
4.a.	What is giga-scale dilemma and short channel effects in modern digital design. Explain how these challenges influence the performance and reliability of integrated circuits.	7
b.	What are FinFET and TFET technologies, and how do they address the giga-scale dilemma?	7
5.a.	Describe the common-source (CS) amplifier stage with resistive load and current source load configurations.	7
b.	Explain the basic differential amplifier design, including the common mode response and the Gilbert cell configuration.	7
6.	Compare basic current mirrors with cascade and active current mirrors in terms of performance.	14
7.	What factors contribute to noise in amplifier circuits, and how can designers minimize noise in their designs?	14
8.	Explain the concept of logic effort in the context of static CMOS and dynamic logic design. How does it influence the speed and power dissipation of dynamic gates?	14

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