QP Code: RA22BTECH401 | Reg. No | | | | | | | | | | | AR 22

Gandhi Institute of Engineering and Technology University, Odisha, Gunupur
(GIET University)

B. Tech (Sixth Semester - Regular) Examinations, April 2025

21BECPC36001 – Digital VLSI Design

(ECE)

Time: 3 hrs | Maximum: 70 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

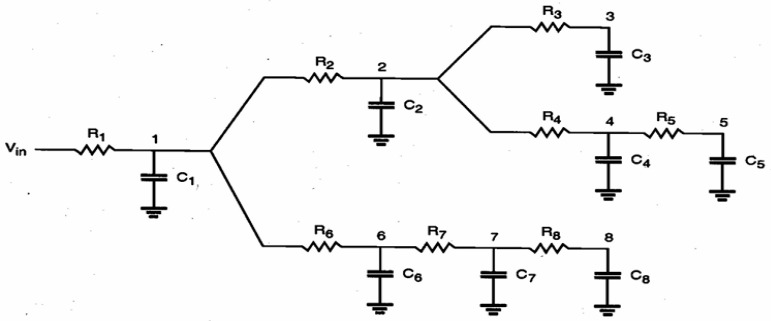
		CO #	Blooms Level
Q.1.	Answer ***ALL*** questions		
a.	Define Moore's Law.	CO1	K1
b.	Define accumulation and inversion region in MOS capacitor.	CO1	K1
c.	Basic difference between a static CMOS and a dynamic CMOS .	CO4	K2
d.	What is the significance of CMOS technology in digital VLSI design?	CO4	K2
e.	Define the noise margin and write the expression noise margin high.	CO3	K2

PART – B **(15 x 4 = 60 Marks)**

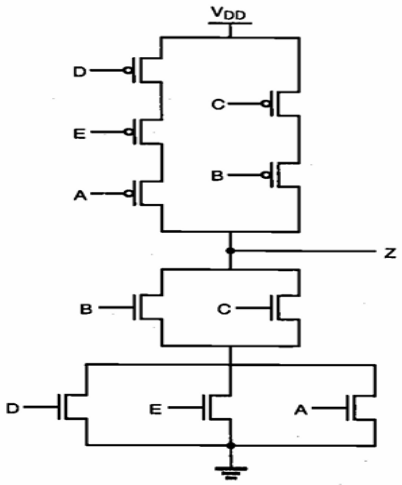
	Answer ***All*** the questions	Marks	CO #	Blooms Level
2. a.	Explain the various VLSI design methodologies. Compare and contrast the Full-Custom, Semi-Custom, and Programmable Logic design approaches in terms of design time, flexibility, performance, and cost.	8	CO2	K4
b.	Explain the structural decomposition of a 4-bit adder. Illustrate the different levels of hierarchy involved in combining individual 1-bit full adders to form the 4-bit adder.	7	CO3	K4
	(OR)			
c.	Describe the fabrication process flow for manufacturing a VLSI (Very-Large-Scale Integration) chip. Discuss the various steps involved, from wafer preparation to packaging.	8	CO1	K1
d.	Explain the behavior of a MOS (Metal-Oxide-Semiconductor) system under external bias. Derive the expressions for the threshold voltage and discuss the effects of various external biases (gate, drain, and source) on the operation of the MOS transistor.	7	CO1	K1
3.a.	Consider a MOS structure comprising a n-type doped silicon substrate, a silicon dioxide layer, and a metal gate. The equilibrium Fermi potential of the doped silicon substrate is $q\emptyset_{Fn}$ = 0.2 eV. Electron affinity of silicon and the metal are 4.15 and 4.1eV respectively. Calculate the built-in potential difference across the MOS system. Draw the Energy band diagrams of the components that make up the MOS system.	8	CO1	K1
b.	Draw the stick diagram of Y=$\overline{(A+B)+C}$	7	CO2	K3
	(OR)			
c.	Design the combinational logic circuit Y=$\overline{A.B.C}$ using CMOS technology	5	CO4	K6
d.	Write the code of SR FF using Verilog code	10	CO4	K6
4.a.	Explain working principle of CMOS transmission gate and find effective resistance of three different region	8	CO4	K4
b.	Derive the values of Derive V_{IH} and V_{OH} for a CMOS inverter.	7	CO3	K4

(OR)

c.	Consider a CMOS inverter circuit with the following parameters: VDD =3.3 V $V_{T,n}$=0.6V,$V_{T,p}$ =-0.7 V k_n = 200 µA/V2 k_p= 80 µA/V2 (5.83) (5.84) Calculate the noise margins of the circuit..	8	CO3	K4
d.	Find the Elmore delay at node 1 node 7	7	CO3	K4

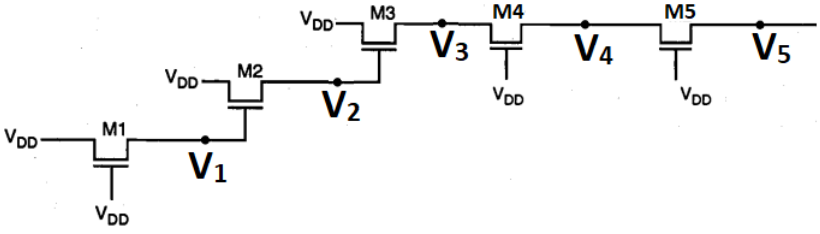


5.a.	Draw the CMOS SR-Latch circuit based on NAND gate and explain its function and write the corresponding truth table	10	CO4	K2
b.	Find an equivalent $(W/L)_P$ and $(W/L)_n$ of CMOS inverter circuit for simultaneous switching of all inputs, assuming that (W/L)p = 5 for all pMOS transistors and (W/L) = 6 for all nMOS transistors.	5	CO3	K3



(OR)

c.	Explain the voltage bootstrapping method and discuss the need for bootstrapping, illustrate the working with a suitable circuit diagram, and derive the expression for the capacitor ratio .$\frac{C_{boot}}{C_x}$	10	CO3	K4
d.	Observe the given circuit and find the voltage V_1, V_2, V_3, V_4, and V_5. Consider the threshold voltage for nMOS transistor M1, M2, M3, M4, and M5 as V_{TH1}, V_{TH2}, V_{TH3}, V_{TH4}, and V_{TH5} respectively.	5	CO3	K4



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