QP Code: RA23BTECH115 | Reg. No | | | | | | | | | | | AY 23

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, ODISHA, GUNUPUR
(GIET UNIVERSITY)

B. Tech (Fourth Semester - Regular) Examinations, April – 2025

23BECPC24001 – Digital System Design
(ECE)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right-hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	Convert 712.5 to binary, hexadecimal and Octal.	CO1	K2
b.	State De Morgan's Theorems.	CO1	K1
c.	Define "Prime Implicants" in a Karnaugh map? Under what condition a min-term in a group is said to be essential?	CO2	K1
d.	State the difference between "latch" and "flip-flop".	CO3	K1
e.	Define Noise Margin and propagation Delay in output waveform of the logic gate.	CO5	K1

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2. a.	Find the following additions: I. (+14, -9) using 1's complement notation. II. (-16, +11) using 2's complement notation.	5	CO1	K3
b.	Express the number (-3.75) as a floating-point number using IEEE single precision.	5	CO1	K2
	(OR)			
c.	Establish the following identities of Boolean algebra (i) A + AB = A (ii) (A+ B)(A+ C) = A+ BC	5	CO1	K2
d.	Implement the following function using NOR gates only. F (A, B, C, D) = (A + C) (B + D).	5	CO1	K2
3.a.	For the given function find the minimized form and implement using basic logic gates. F = Σ m (1, 3, 5, 7, 9, 15) + d (4, 6, 12, 13)	5	CO2	K3
b.	A magnitude comparator is a combinational circuit that compares two numbers, A and B, and determines their relative magnitudes. The outcome of the comparison is specified by three binary variables that indicate whether A>B, A=B or A < B. Determine the algorithm to implement this comparator and draw a 2-bit magnitude comparator using combinational circuit.	5	CO2	K3
	(OR)			
c.	What is an encoder? Design an Octal-to-Binary encoder.	5	CO2	K3
d.	The four variable logic function can be expressed as F (A, B, C, D) = Σ m (1, 2, 5, 7, 9, 11, 14). Realize the above function using 8 x 1 MUX.	5	CO2	K3
4.a.	Explain how a J-K flip-flop can be constructed using D flip-flop.	5	CO3	K6
b.	An 8-bit shift register has the binary equivalent of the decimal number 98 stored in it. Find the base-10 equivalent contents of the register after the following	5	CO3	K2

operations have been performed? For each case, assume the same initial state given.

(i) Shift Left 1
(ii) Shift Right 1
(iii) Rotate Right 2
(iv) Rotate Left 2

(OR)

c.	State shift Registers types. Explain the principle of a 4-bit Serial-in Parallel-out shift register with required diagram.	5	CO3	K2
d.	Define race around conditions in JK flipflop and explain how it is avoided by using master slave Flip-flop with its circuit diagram.	5	CO3	K4
5.a.	Draw the diagram of the 4 × 4 RAM.	5	CO4	K2
b.	Design a Decade counter using D-flip flops.	5	CO3	K3

(OR)

c.	Design a Full Adder circuit using a ROM.	5	CO4	K3
d.	Design a synchronous counter for the following sequence using T flip-flops: 1, 3, 5, 6, 1,	5	CO3	K3
6.a.	Design the Boolean expression F= (ABC+DE)' using CMOS Logic.	5	CO5	K3
b.	Write a VHDL code for the 4-bit equality detector using Data Flow modelling	5	CO6	K6

(OR)

c.	Write a short note on **any one** of the following: (a) CMOS Inverter (b) DTL NAND.	5	CO5	K2
d.	Write a VHDL code for the 2×1 MUX using Behavioral modelling.	5	CO6	K6

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