QP Code: RA23BTECH121 Reg. No | | | | | | | | | | | AY 23

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY, ODISHA, GUNUPUR
(GIET UNIVERSITY)

B. Tech (Fourth Semester - Regular) Examinations, April – 2025

23BCSPC24002/23BCMPC24002/23BCDPC24002
Computer Organisation and Architecture

(CSE, AI&ML, DS)

Time: 3 hrs Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions	CO #	Blooms Level
a. What is the use the following registers in a CPU: PC, MAR	CO1	K2
b. Write the addressing mode of the following instructions. MOV R1, #25 , LD R0, 250	CO2	K2
c. Represent the number 11010.1011 $\times 2^4$ in single precision method.	CO3	K3
d. Classify architecture according to Flynn's classification.	CO4	K1
e. Write the difference between logical address and physical address.	CO5	K2

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions	Marks	CO #	Blooms Level
2. a. What is performance of a computing system? How it can be improved?	5	CO1	K1
b. Write assembly language program to find the addition of 10 data bytes which are stored in memory having starting address ADR1 onwards.	5	CO2	K3
(OR)			
c. Define Byte addressability in memory. Explain each type with examples.	5	CO1	K1
d. Write assembly language program to find the smallest number of the given 15 data bytes which are stored in memory from LOC1 to LOC15.	5	CO2	K3
3.a. Divide 16 by 6 using restoring division algorithm.	5	CO3	K2
b. Design n-bit ripple carry adder/ subtractor and analyse its performance.	5	CO3	K4
(OR)			
c. Multiply 17 with 9 using Fast multiplication methd.	5	CO3	K2
d. Represent the following numbers in single precession IEEE standard format (i) -14.25 (ii) 11010.111001$\times 2^5$	5	CO3	K3
4.a. What is pipeline architecture? Write the advantages and disadvantages of implementing it .	5	CO4	K1
b. Write the different steps with control signals generated during execution of ADD R1, (R2) in multiple organization.	5	CO4	K2
(OR)			
c. Differentiate between hardwired control unit and microprogrammed control unit.	5	CO4	K2
d. Define Hazard. How do different hazards occur? Explain with example.	5	CO4	K1
5.a. Distinguish between SRAM and DRAM cell.	5	CO5	K2

b.	Draw and explain the Hard Disc structure.	5	CO5	K1
	(OR)			
c.	How different cache mapping functions are used in cache memory? Explain with example.	8	CO5	K2
d.	Let us consider a system having cache access time 0.5 ns, hit ratio 60%, main memory access time is 100 ns. Then find out performance of system with cache.	2	CO5	K3
6.a.	What is virtual memory? How does it do memory management ?	5	CO5	K1
b.	Define interrupt. Discuss about its classification in computer system.	5	CO5	K1
	(OR)			
c.	Add and multiply the following two floating point numbers by using IEEE Standard rule: 10.125 and 7. 05	5	CO3	K2
d.	Explain the term ISA in assembly language program.	5	CO1	K1

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