QP Code: RN23BTECH047 | Reg. No | | | | | | | | | | | AY 23

GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR
(GIET UNIVERSITY)

B. Tech (Third Semester - Regular) Examinations, November – 2024

23BCSES23003/23BCMES23001/23BCDES23001 – DIGITAL ELECTRONICS

(CSE-AIML,DS,CSE)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	Convert 712.5 to binary, hexadecimal and Octal.	CO1	K2
b.	State De Morgan's Theorems.	CO3	K1
c.	Define "Prime Implicants" in a Karnaugh map? Under what condition a min-term in a group is said to be essential?	CO4	K1
d.	State the difference between "latch" and "flip-flop".	CO5	K1
e.	Draw PIPO Register.	CO6	K1

PART – B **(10 x 5 = 50 Marks)**

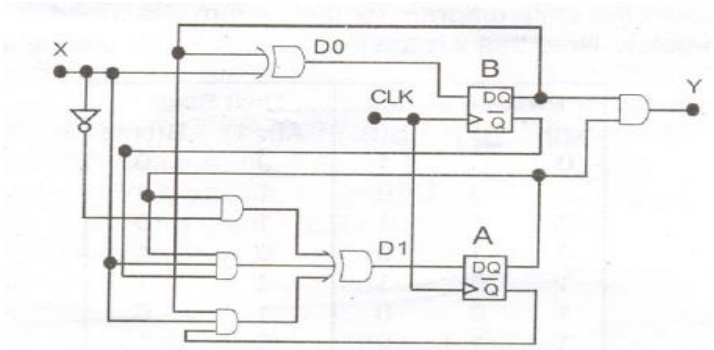
Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2. a.	Find the following additions: I. (+14, -9) using 1's complement notation. II. (-16, +11) using 2's complement notation.	5	CO2	K3
b.	State consensus Theorem and show that: AB+AB'C+BC'=AC+BC'	5	CO3	K1
	(OR)			
c.	List the "2421" code and "Excess-3" code of decimal digit "0 to 9"in a Tabular form. What are the special properties of these codes?	5	CO2	K1
d.	Mention the IEEE 754 format for the double precision method and Express the number (-3.75) as a floating-point number using IEEE single precision.	5	CO2	K2
3.a.	For the given function find the minimized form and implement using basic logic gates. $F = \Sigma m (1, 3, 5, 7, 9, 15) + d (4, 6, 12, 13)$	5	CO4	K3
b.	Write short notes on **any two** of the following: a) Binary Multiplier b) Magnitude Comparator c) Decoder d) Encoder	5	CO4	K1
	(OR)			
c.	Define Full adder and design it using two half adder circuits and 'OR' gate.	5	CO4	K3
d.	The four variable logic function can be expressed as $F (A, B, C, D) = \Sigma m (1, 2, 5, 7, 9, 11, 14)$. Realize the above function using 8 x 1 MUX.	5	CO4	K3
4.a.	Explain how a J-K flip-flop can be constructed using D flip-flop.	5	CO5	K6
b.	Differentiate between Mealy and Moore models.	5	CO5	K4

Construct the state diagram for the system described in the state table given below. Note that x is the input and A & B are the state variables.

	Present Values		Next State	
x(t)	A(t)	B(t)	A (t+1)	B (t+1)
0	0	1	0	0
0	0	0	1	1
0	1	1	1	0
0	1	0	0	1
1	0	1	1	1
1	0	0	1	0
1	1	0	0	1
1	1	1	0	0

(OR)

c. Derive the next state, the output table and the state diagram for the sequential circuit shown in the Figure below:



5 CO5 K3

d. Define race around conditions in JK flipflop and explain how it is avoided by using master slave Flip-flop with its circuit diagram. 5 CO5 K2

5.a. State shift register types. Explain the principle of a 4-bit Serial-in Parallel-out shift register with required diagram. 5 CO6 K2

b. Design a Decade counter using D-flip flops. 5 CO6 K6

(OR)

c. An 8-bit shift register has the binary equivalent of the decimal number 86 stored in it. Find the base-10 equivalent contents of the register after the following operations have been performed? For each case, assume the same initial state given.

(i) Shift Left 1
(ii) Shift Right 2
(iii) Rotate Right 2
(iv) Rotate Left 2

5 CO6 K5

d. Design a synchronous counter for the following sequence using T flip-flops: 1, 3, 5, 6, 1, 5 CO6 K3

6.a. How many 32K × 8 RAM chips are needed to provide a memory capacity of 256 K bytes? How many lines of the address must be used to access 256K bytes? How many of these lines are connected to the address inputs of all chips? 5 CO6 K3

b. Design a combinational circuit using a ROM. The circuit accepts a three-bit number and outputs a binary number equal to the square of the input number. 5 CO6 K6

(OR)

c. Differentiate between Static RAM and Dynamic RAM. 5 CO6 K2

d. A 3-input majority circuits produces the output as '1' when the number of 1's are more than the number of 0's at the input. Implement it using ROM. 5 CO6 K6

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