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GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR

(GIET UNIVERSITY)

M.Tech. (First Semester) Regular Examinations, February – 2025

24MVLPC11002 –Digital IC Design

ECE(VLSI Design)

Time: 3 hrs | Maximum: 60 Marks

Answer ALL questions

(The figures in the right hand margin indicate marks)

PART – A **(2 x 5 = 10 Marks)**

Q.1. Answer ***ALL*** questions		CO #	Blooms Level
a.	What are the major challenges associated with dynamic logic design?	CO1	K2
b.	How does a clocked flip-flop differ from a latch in terms of operation and functionality?	CO2	K1
c.	What is the difference between the data path and control path in a processor?	CO3	K1
d.	What are the primary components that make up the data path in a processor?	CO4	K1
e	What are the different types of logic gates used in CMOS circuits?	CO2	K2

PART – B **(10 x 5 = 50 Marks)**

Answer ***ALL*** the questions		Marks	CO #	Blooms Level
2. a.	Explain the structure and functionality of the following circuits: (i) Data path circuit (ii) Any one type of adder circuit	5	CO1	K2
b.	Describe the working principle, architecture, and operational impact of an SRAM cell on memory performance.	5	CO1	K3
	(OR)			
c.	Compare enhancement mode and depletion mode MOSFETs, discussing their electrical behavior, threshold voltage differences, and applications in analog and digital circuits.	5	CO1	K1
d.	Illustrate and explain the stick diagram and physical layout of an NMOS inverter, emphasizing design steps and layout constraints.	5	CO1	K3
3.a.	What are ratioed circuits and dynamic CMOS logic configurations? Discuss their advantages, disadvantages, and real-world applications.	5	CO2	K2
b.	Explain the concept of accumulation mode in semiconductor devices and its significance in MOS capacitor behaviour.	5	CO2	K4
	(OR)			
c.	How does sequencing impact dynamic circuits? Discuss its importance in clocking schemes, power consumption, and high-speed digital design.	5	CO2	K4
d.	Compare and contrast different types of adder circuits used in digital design, such as the Ripple Carry Adder, Carry Look ahead Adder, and Booth Adder.	5	CO2	K3
4.a.	Describe the structure, operation, and benefits of a Booth multiplier in digital arithmetic computations.	5	CO3	K2
b.	What are the key design considerations for an NMOS inverter layout? Explain in brief	5	CO3	K3
	(OR)			

c.	Explain the significance of differential signalling in high-speed communication systems and how it improves signal integrity.	5	CO3	K2
d.	Describe the role of substrate biasing in semiconductor devices, explaining its impact on threshold voltage and device efficiency.	5	CO3	K3
5.a.	Explain the working principle of a pass transistor logic circuit, comparing its advantages and limitations with traditional CMOS logic.	5	CO4	K4
b.	Analyze the 6-transistor (6T) SRAM cell, explaining its configuration, stability, and read/write operations in memory circuits.	5	CO4	K3
	(OR)			
c.	Discuss the impact of sequencing techniques in dynamic circuit design, focusing on timing, clock skew, and power efficiency in high-performance circuits.	5	CO4	K1
d.	Explain the concept of charge sharing in dynamic logic circuits, detailing its impact on circuit stability and possible mitigation techniques.	5	CO4	K2
6.a.	Describe the concept of leakage current in MOSFETs, analyzing its sources, impact on low-power design, and techniques to minimize leakage in modern VLSI circuits.	5	CO2	K3
b.	Compare a latch and a flip-flop in terms of functionality, timing characteristics, and their role in sequential circuits.	5	CO1	K3
	(OR)			
c.	Evaluate the advantages and disadvantages of latches in electronic circuits, considering factors such as power efficiency, speed, and area consumption.	5	CO1	K1
d.	Explain the significance of Booth multiplication in digital systems. How does its structure contribute to computational efficiency?	5	CO3	K3

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