**GANDHI INSTITUTE OF ENGINEERING AND TECHNOLOGY UNIVERSITY, ODISHA, GUNUPUR**
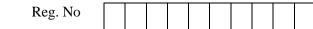**(GIET UNIVERSITY)**
Ph.D. (First Semester) Examinations, December – 2024
**23SPPEEC1012 – Analog and Digital CMOS VLSI Design**
(ECE)

Time: 3 hrs                                                                                   Maximum: 70 Marks

**The figures in the right hand margin indicate marks.**

**Answer *ANY FIVE* Questions.**                    **(14 x 5 = 70 Marks)**    **Marks**

| | | |
|---|---|---|
| 1.a. | Explain the basic structure of a Metal-Oxide-Semiconductor (MOS) transistor and its characteristics with applied bias of ($V_g > 0$, $V_g < 0$). | 8 |
| b. | What are the key quality metrics in digital design, and how does each metric impact the overall performance of a circuit? | 6 |
| 2. | Discuss the static and dynamic characteristics of CMOS inverter, and how to evaluate its switching threshold, noise margin and power consumption? | 14 |
| 3.a. | Define a stick diagram, and draw the stick diagram for an CMOS inverter and discuss its importance in the layout design process. | 7 |
| b. | Explain the process of clock tree synthesis (CTS) and its importance in digital design. | 7 |
| 4. | Compare and contrast static CMOS design, ratioed logic, and pass transistor logic. | 14 |
| 5. | Explain the bi-stability principle in static latches and registers. Describe dynamic latches and registers, including their advantages and disadvantages | 14 |
| 6.a. | What is pipelining, and how does it enhance the performance of sequential circuits? | 7 |
| b. | Discuss the challenges posed by short channel effects in advanced MOS technologies. | 7 |
| 7. | Explain the concept of logic effort in the context of static CMOS and dynamic logic design. How does it influence the speed and power dissipation of dynamic gates? | 14 |
| 8. | Discuss the frequency response of different amplifier stages (CS stage, source follower, common gate stage) and their implications for circuit design. | 14 |

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